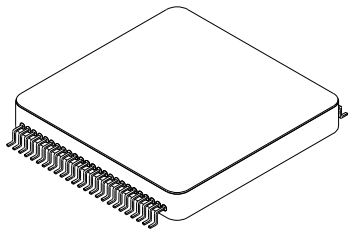
MIL-PRF-38534 CERTIFIED FACILITY

RAD HARD LOW VOLTAGE 10A SWITCHING REGULATOR WITH CURRENT SHARE

5061RH

FEATURES:

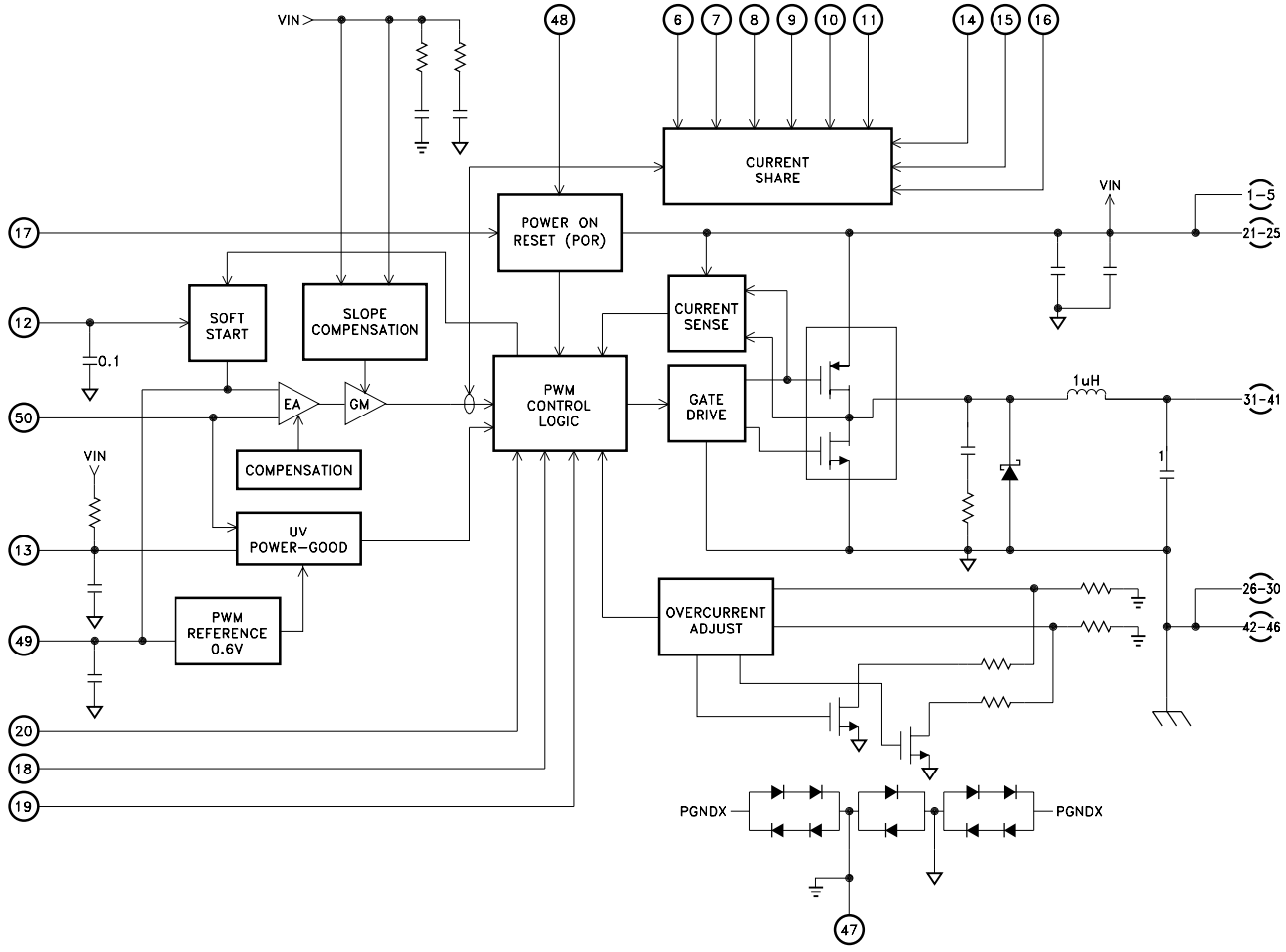


- Radiation Hardened to 100Krad, High and Low Dose Rates
- Exceptional SEE Performance
- TOR Ready, Designed and Derated to MIL-STD-1547B and NASA EEE-INST-002
- Integrated Inductor
- Adjustable 0.6V to 4.0V Output, Greater than 10A
- 2 Phase Current Sharing Mode Enables Output Current in Excess of 20A
- Adjustable Frequency and Synchronization for Sensitive Applications
- Soft-Start, Logic Level Enable, PGOOD Flag, and Power On Reset Features Simplify Sequencing
- Simple Heat Sinking; Low Thermal Resistance, Pin Connected Case
- Contact TTM Technologies for MIL-PRF-38534 Qualification status.

DESCRIPTION:

The MSK5061RH is a radiation hardened adjustable output switching voltage regulator. The wide input and output range, output current in excess of 10A, and full complement of features defines this regulator as an ideal solution for many space power applications. Designed specifically for the cutting edge low voltage/high current FPGA & ASIC technologies, two MSK5061RH can be operated in 2 phase current sharing mode to deliver output currents in excess of 20A accross the full output range. The robust integrated inductor and passives significantly reduce design time and board area. All internal components have been designed to satisfy even the most stringent reliability requirements, mitigating program design-in risks. The MSK5061RH is hermetically sealed in a 50 pin flatpack.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Low Voltage High Current Point of Load Regulation
- High Efficiency Satellite and space craft power supply
- High power FPGA, ASIC, µP, & Analog POL

PIN-OUT INFORMATION

1	VIN1	26	PGND1/CASE
2	VIN2	27	PGND2
3	VIN3	28	PGND3
4	VIN4	29	PGND4
5	VIN5	30	PGND5
6	ISHA	31	VOUT1
7	ISHREFA	32	VOUT2
8	ISHB	33	VOUT3
9	ISHREFB	34	VOUT4
10	ISHC	35	VOUT5
11	ISHREFC	36	VOUT6
12	SS	37	VOUT7
13	PGOOD	38	VOUT8
14	ISHCOM	39	VOUT9
15	ISHSL	40	VOUT10
16	ISHEN	41	VOUT11
17	PORSEL	42	PGND6
18	SYNC	43	PGND7
19	M/S	44	PGND8
20	FSEL	45	PGND9
21	VIN6	46	PGND10
22	VIN7	47	AGND
23	VIN8	48	EN
24	VIN9	49	REF
25	VIN10	50	FB

ABSOLUTE MAXIMUM RATINGS ⑥

V_{IN} Supply Voltage 6.2V
I_{OUT} Output Current ..⑧..... 14A
T_C Case Operating Temperature Range
MSK5061K/HRH ..... -55°C to +125°C
MSK5061RH ..... -40°C to +85°C

T_{ST} Storage Temperature Range.....-65°C to +150°C
T_{LD} Lead Temperature Range
(10 Seconds) ..... 300°C
T_J Junction Temperature ..... 150°C
ESD Rating ..... Class 2

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ① ⑦		Group A Subgroup	MSK5061K/HRH Min.	Typ.	Max.	Units
Operating Supply Current	3.0 ≤ VIN ≤ 5.5V		1, 2, 3	-	0.06	0.11	A
Standby Supply Current (Current Share Disabled)	VIN = 5.5V, EN = GND		1, 2, 3	-	2.5	6	mA
	VIN = 3.6V, EN = GND ②		1, 2, 3	-	2	-	
Standby Supply Current ② (Current Share Enabled, Slave)	VIN = ISHEN = ISHSL = 5.5V EN = M/S = GND, SYNC = 1MHz		1, 2, 3	-	2.5	7	mA
			1, 2, 3	-	2	11	
Reference Voltage	3.0 ≤ VIN ≤ 5.5V		1, 2, 3	0.594	0.6	0.606	V
Error Amp Input Offset Voltage ②	VIN = 5.5V		1, 2, 3	-1	-	3	mV
FB Pin Input Leakage	VIN = 5.5V		1, 2, 3	-1.5	-	1.5	uA
Internal Oscillator Frequency (SYNC)	3.0 ≤ VIN ≤ 5.5V, M/S = VIN	FSEL = VIN	4, 5, 6	0.85	1	1.15	MHz
		FSEL = GND	4, 5, 6	0.425	0.5	0.575	MHz
External Oscillator Synchronization Range	3.0 ≤ VIN ≤ 5.5V SYNC = 0.4MHz TO 1.2MHz		7, 8A, 8B	-	-	-	P/F
SYNC Pin Input High Voltage Threshold	M/S = GND		1, 2, 3	2.3	1.7	-	V
SYNC Pin Input Low Voltage Threshold	M/S = GND		1, 2, 3	-	1.5	1	V
SYNC Pin Output Voltage ②	3.0 ≤ VIN ≤ 5.5V		1, 2, 3	-	0.1	0.4	V
	3.0 ≤ VIN ≤ 5.5V		1, 2, 3	-	0.1	0.4	V
Minimum LX On Time ②	VIN = 5.5V		4, 5, 6	-	200	275	nS
Minimum LX Off Time ②	VIN = 5.5V		4, 5, 6	-	0	50	nS
Minimum LX On Time ②	VIN = 3V		4, 5, 6	-	225	300	nS
Minimum LX Off Time ②	VIN = 3V		4, 5, 6	-	0	50	nS
Logic Pin Voltage Threshold ② (PORSEL, M/S, ISHSL, ISHEN, FSEL, SYNC)		Input High Threshold	1, 2, 3	VIN - 0.5	1.3	0.5	V
		Input Low Threshold	1, 2, 3	-	1.3	0.5	uA
Logic Pin Input Leakage ② (PORSEL, M/S, ISHSL, ISHEN, FSEL, SYNC)	VIN = 5.5V		1, 2, 3	-1	-	1	uA
VIN Power On Reset Rising Threshold	PORSEL = VIN		1, 2, 3	4.1	4.3	4.45	V
	PORSEL = GND		1, 2, 3	2.65	2.8	2.95	
VIN Power On Reset Hysteresis	PORSEL = VIN		1, 2, 3	225	325	425	mV
	PORSEL = GND		1, 2, 3	40	140	240	
Enable (EN) Input Voltage Threshold			1, 2, 3	0.56	0.6	0.64	V
Enable (EN) Leakage Current	VIN = EN = 5.5V		1, 2, 3	-3	-	3	V
Enable (EN) Sink Current	VIN = 5.5V, EN = 0.3V		1, 2, 3	6.4	11	16.6	uA
SS Pin Charging Current	3.0 ≤ VIN 5.5V, SS = GND		1, 2, 3	20	23	27	uA
SS Pin Discharge On Resistance ②	3.0 ≤ VIN 5.5V, EN = GND		1, 2, 3	-	2.2	4.7	Ω
PGOOD Sink Current	VIN = 3.0V, PGOOD = 0.4V, EN = GND		1, 2, 3	6	-	-	mA
PGOOD On Voltage	VIN = 5.5V		1, 2, 3	5.25	5.5	-	V
Current Limit, Running	VIN = 3.3V, FSEL = GND		1, 2, 3	10	11.5	13	A
Current Limit, SoftStart	VIN = 3.3V, FSEL = GND		1, 2, 3	11	12.5	14	A
		POST IRRADIATION	1	11	12.5	14.5	A
Current Sharing Ratio	Iout Slave/Iout Master	IOUT = 5.0A	1, 2, 3	0.5	1	1.5	A/A
VOUT Regulation, Four Corner	3.0 ≤ VIN ≤ 5.5V 0A ≤ ILOAD ≤ 10A Referenced to VOUT at VIN = 4.25V, Iload = 5A		1, 2, 3	-0.5	-	0.5	%
VOUT Ripple Voltage ②	3.0 ≤ VIN ≤ 5.5V 20MHz Bandwidth COUT ESR = 5mΩ at 1MHz		1, 2, 3	-	5	10	mVpp
Efficiency	VIN = 5V, VOUT = 3.3V IOUT = 5A		1, 2, 3	85	90	-	%
Thermal Resistance ②	Junction to case @ 125°C Power Switches		-	-	1.8	2.1	°C/W

NOTES:

① Unless otherwise specified VIN = 5.5V, VOUT=1.5V, LOAD = 2.5K, 1MHz, current share disabled.

② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.

③ Industrial grade devices shall be tested to subgroup 1 and 4 unless otherwise specified.

④ Military and space grade devices ('H' and 'K' suffix) shall be 100% tested to Subgroups 1,2,3 and 4.

⑤ Subgroup 5 and 6 testing available upon request.
Subgroup 1, 4, 7 TA = TC = +25°C
Subgroup 2, 5, 8A TA = TC = +125°C
Subgroup 3, 6, 8B TA = TC = -55°C

⑥ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.

⑦ Pre and post irradiation limits @ 25°C, up to 100Krad TID, are identical unless otherwise specified.

⑧ Absolute maximum output current rating is subordinate to the "RMS output current vs case temperature" SOA curve on sheet 8.

APPLICATION NOTES

PIN FUNCTIONS

VIN – The VIN pins are the input supply pins for all of the internal circuitry. High di/dt switching currents are conducted through these pins. Locally decouple VIN to PGND with a mix high frequency ceramic capacitors and low ESR tantalum. Provide sufficient bulk capacitance to ensure a low impedance buss and limit input voltage ripple.

PGND – The PGND pins connect to the internal power ground plane. High di/dt switching currents are conducted through these pins. Provide a continuous low impedance ground path between the MSK5061RH PGND, the input supply return, and the load. Avoid layouts that force load return current to cross the AGND reference path.

VOUT – The VOUT pins are connected to the internal output inductor. Connect VOUT as close as possible to the load to minimize bus impedance. Connecting 500 to 1000µF low ESR bulk capacitance to VOUT is typically sufficient to ensure stable operation. Some ceramic capacitance near the load is typically required to roll off high frequency gain, suppress switching noise and fast load transients. A mix of high frequency ceramic capacitors and low ESR tantalum are recommended. See Output Capacitor Selection paragraph.

AGND – The AGND pin provides a low noise signal reference for the internal control circuitry. For optimum regulation performance, connect AGND and PGND together near the ground side of the load.

PGND1/CASE – This pin is electrically connected to the MSK5061RH case and PGND.

FB – The FB pin is the inverting input to the error amplifier. The voltage at this pin and the 0.6V reference voltage are used to servo to current control loop set point. Place a resistor divider between VOUT and AGND near the load, and connect the FB pin to the center node to program the output voltage. See Output Voltage Selection paragraph.

REF – The REF pin is the internal 0.6V reference voltage used in several circuit functions. The reference voltage is pined out for current sharing applications. When applying the 2 phase current sharing functionality, connect the REF pins of the master and slave MSK5061RHs through a 10Ω resistor. This pin must not be otherwise loaded.

FSEL – The FSEL pin is used to program the Switching frequency of the MSK5061RH. Connect to VIN for 1MHz or to PGND for 500KHz operation.

PORSEL – The PORSEL pin is used to program the power on reset thresholds of the MSK5061RH. Connect to VIN for a 5V nominal input bus, or PGND for a 3.3V nominal input bus. Connect to PGND for a input bus that varies from 3V to 5.5V.

SS – The Soft Start pin provides control of turn on surge currents and enables coincident or ratiometric tracking functionality. A 23µA current source charges the internal SS capacitor and sets the output ramp rate to approximately 2.6mS. Connect additional capacitance to reduce the output ramp rate. In 2 phase current sharing applications, the slave ramp rate should be at least twice that of the master. Further application guidance is provided in the Start Up Considerations section.

EN – The EN pin provides hysteretic on/off control of the regulator. Driving this pin above 0.6V enables the regulator. Programmable hysteresis is realized with an 11µA current sink that is active until the pin voltage exceeds VREF. Bypass with a capacitor to ground when controlling from a high impendence source. See the applications section for further guidance.

PGOOD – The PGOOD pin is a high impedance logic output that is pulled low when the regulators output voltage is outside of a ±11% typical window. This status flag can be used for supply sequencing and fault detection.

M/S – The M/S input pin determines the function of the bidirectional SYNC pin. Connect M/S to VIN for Master mode, where the SYNC pin is the master oscillator output. Connect M/S to PGND for Slave mode, where SYNC becomes an input.

SYNC – When SYNC is configured as an output, M/S = VIN, this pin drives the SYNC pin input of another MSK5061RH with a square wave that is phase shifted ≈180° from the Master clock driving the Master PWM circuits. When configured as an input, M/S = PGND, this pin uses the SYNC output from another MSK5061RH or an external clock to clock the PWM circuitry. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 400kHz to 1.2MHz.

ISHEN – The ISHEN pin enables the current sharing feature. Connect to VIN to enable current sharing functions. Connect to PGND to disable the current sharing features.

ISHSL – The ISHSL pin configures the MSK5061RH as either a current share master or slave. Connect to PGND to configure the device as a master or if current sharing functions are not implemented. Connect to VIN to configure the MSK5061RH as a current share slave device.

ISHCOM – ISHCOM is a bidirectional communication line between a current share Master and a current share Slave. If using current share, tie ISHCOM of the Master to ISHCOM of the Slave. The Master enables the Slave by resistively (~ 8.5kΩ) pulling ISHCOM high. The Slave indicates an over-current fault condition to the Master by pulling ISHCOM low. To mitigate SET, connect a 47pF ceramic capacitor from ISHCOM to the PWB ground plane. If not using current share this pin should be floated or connected to the PCB ground plane. ISHCOM is tri-stated if ISHEN is low.

ISHREFA, B, C - If configured as a current share Master the ISHREFA/ISHREFB/ISHREFC pins provide a reference output current equal to 100µA each. If configured as a current share Slave, the ISHREFA/ISHREFB/ISHREFC pins accept a reference input current. For a current share Slave, this input current is used together with the ISHA/ISHB/ISHC current to determine the Master's redundant A/B/C error amp output current. If using current share, tie ISHREFA/ISHREFB/ISHREFC of the MASTER to ISHREFA/ISHREFB/ISHREFC of the Slave. If not using current share, tie ISHREFA/ISHREFB/ISHREFC to VIN. The purpose of the reference current is to reduce the impact of external noise coupling onto ISHA/ISHB/ISHC. ISHREFA/ISHREFB/ISHREFC are tri-stated prior to a valid POR and when ISHEN = PGND.

ISHA, B, C – If configured as a current share Master, the ISHA/ ISHB/ISHC pins are outputs that provide a current equal to 25 times the redundant A/B/C error amp output currents plus ISHREFA/ ISHREFB/ISHREFC (nominally 100µA each). If configured as a current share Slave, the ISHA/ISHB/ISHC pins are inputs that become the Slave's redundant A/B/C error amp output current. If using current share, tie ISHA/ISHB/ISHC of the Master to ISHA/ ISHB/ ISHC of the Slave. If not using current share, tie ISHA/ISHB/ ISHC to DVDD. ISHA/ISHB/ISHC are tri-stated prior to a valid POR and when ISHEN = PGND.

POWER SUPPLY BYPASSING

Current is drawn from the input bus in roughly trapezoidal pulses with very fast edge rates, and consequently consists of a broad frequency spectrum. High quality low ESR/ESL ceramic capacitors connected directly across the VIN and PGND pins are recommended to provide a low impedance to the high frequency components of the wave form and trap them local to the regulator, thereby limiting conducted EMI. Minimizing the area of the VIN-CIN-PGND loop will help minimize radiated EMI. The MSK5061RH simplifies application with the inclusion of significant internal ceramic capacitance. The internal and external input capacitors source the AC component of the switched current into the regulator. The RMS ripple current seen by the input capacitors is high, approaching a maximum of 0.5 x Iout at approximately 50% duty cycle. Sufficient bulk capacitance must be provided to minimize ripple voltage seen by the device and ensure stable operation. As a general rule of thumb, VIN ripple should be less than 3 to 5% of VIN. Selection of the bulk input capacitors will likely involve a parallel combination of several tantalum and ceramics to allow proper voltage and ripple current derating. Satisfying those requirements will almost invariably result in sufficient bulk to minimize ripple voltage and ensure stable operation.

OUTPUT CAPACITOR SELECTION

When operated at 1MHz, 500uF total of low ESR capacitance mounted near the MSK5061RH have been shown to provide good stability margins. However physical and practical realities may necessitate at least some bypass capacitance local to the load. The capacitor parasitic ESR and ESL, the non-zero impedance between the regulator output and the load terminals, and finite bandwidth will cause a transient voltage signal to develop proportional to the magnitude of the load step. Additional low ESR output capacitance can help mitigate the transient voltage excursions. Care should be exercised in capacitor selection such that the loop maintains adequate stability margin. Additional output capacitance will be required to lower the loop bandwidth and improve stability margins if operating at switch frequencies below 750kHz. Adding 220µF to 330µF is typically a sufficient adjustment for this scenario. See the typical performance curves for addition information.

Resistors in the 1KΩ to 5KΩ range are typically used to minimize power and leakage current effects. Some loop compensation can be achieved by placing R –C networks in parallel with either R1 and/or R2. Any compensation efforts should be verified by analysis and measurement.

OUTPUT VOLTAGES SELECTION

The output voltage is governed by the following equation:

$$V_{OUT} = V_{REF} \times \left[1 + \frac{R1}{R2}\right]$$

Solving for R1:

$$R1 = R2 \times \left[\frac{V_{OUT}}{V_{REF}} - 1\right]$$

START UP CONSIDERATION; POR, EN, SS AND PGOOD

The input of any buck switching regulator exhibits a negative input resistance; i.e. as input voltage decreases the input current increases. Also the current required to charge the output capacitors is proportional to the total output capacitance and the rate at which the output voltage is allowed to rise. At start up a lockup condition can occur in intermediate power systems not designed specifically to handle these additional currents. Further complicating matters is the fact many FPGA, ASIC, and µProcessor place strict constraints on the rise time and sequence of supply rail voltages. The MSK5061RH has several features specifically designed to simplify managing these challenges.

The Power On Reset function prevents the MSK5061RH from initiating the soft start cycle until VIN has risen above the threshold determined by the PORSEL pin strap. Review the Electrical Specifications Table and the pin functional description for guidance in selecting the appropriate POR threshold for your application.

The EN pin enables the regulator output when driven above VREF, providing a convenient means for implementing supply sequencing. Noise immunity is afforded by the user programmable EN pin Hysteresis. Connect the control signal to EN through a resistor divider. An 11µA current source is active until the EN pin voltage crosses 0.6V, creating the upper bound of the hysteresis loop. The current source is disabled once EN exceeds 0.6V, establishing the lower bound of the hysteresis loop. Use the following equations to define the EN pin thresholds and hysteresis.

$$V_{ENABLE} = \left(V_{REF} \times \left[1 + \frac{R_T}{R_B}\right]\right) + \left[I_{EN} \times R_T\right]$$

$$V_{DISABLE} = V_{REF} \times \left[1 + \frac{R_T}{R_B}\right]$$

$$EN_{HYST} = V_{ENABLE} - V_{DISABLE}$$

Once the POR and EN thresholds have been satisfied, a soft start cycle will be initiated. The Soft Start circuit limits the surge current drawn to charge the output capacitors by controlling the ramp rate of the output voltage. This feature can also be exploited to implement coincident and ratiometric tracking supplies required by many cutting edge digital systems. During start up the error amplifier reference voltage is clamped to the SS pin while a 23µA current source charges the SS pin capacitor. The soft start ramp rate can be adjusted over a range of 2.6ms to 214ms. Determine the desired ramp rate and use the following equation to select the corresponding soft start capacitor.

$$C_{SSEXT} = \frac{T_{SS} \times I_{SS}}{V_{REF}} - 0.1\ uF$$

Once the SS pin voltage equals the reference voltage, the clamp is released and the SS pin voltage continues to rise to ≈1.4V. Once the SS pin reaches 1.4V and the output voltage is with ≈±10% of the set point, the PGOOD pin will transition to the high state. After an over current or under voltage fault, the SS pin is discharged through a 2.2Ω nominal resistance.

SYNCHRONIZATION

The MSK5061RH can be externally synchronized to an external clock in the range of 400kHz to 1.2MHz. This gives designers of precision systems the ability to steer switching noise away sensitive bands, reduce supply ripple current, and eliminate power supply beat frequencies generated by multiple free running switching regulators. To synchronize the MSK5061RH to another MSK5061RH simply connect the M/S pins of the master and slave devices to VIN and PGND respectively and directly connect the SYNC pins. Similarly one or more MSK5061RH can be synchronized to a RAD HARD clock generator.

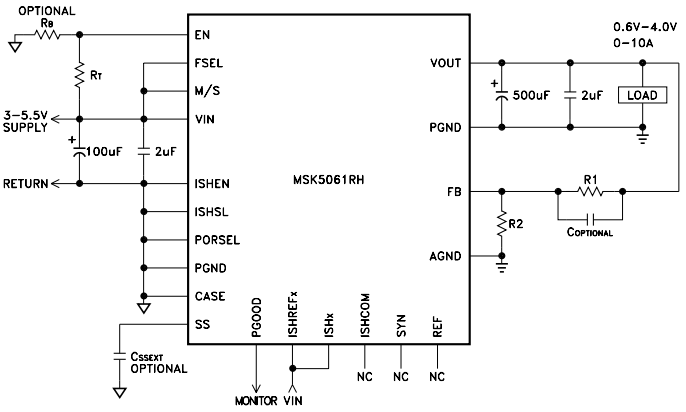
CURRENT SHARING

Two MSK5061RH can be configured together in a robust fault tolerant two phase supply with current capacity in excess of 20A. In this mode, a redundant Current Sharing bus balances the load current between the two devices and communicates any fault conditions. One MSK5061RH is designated the Master and the other the Slave. The Master ISHSL pin is connected to PGND and the Slave ISHSL pin is connected to VIN. The ISHEN pins on both Master and Slave are connected to VIN. The SYNC, ISHA, ISHB, ISHC, ISHREFA, ISHREFB, ISHREFC, ISHCOM and FB pins are connected from the Master to the Slave and the REF pins are tied with a 10Ω resistor. Configured this way, the 2 phase current regulator nearly doubles the load current capacity, limited only by the Current Share Match tolerance. In this Master/ Slave configuration the MSK5061RH operate 180° out-of-phase to minimize the input ripple current, effectively operating as a single IC at twice the switching frequency. Also under idealized conditions the output ripple voltage terms can completely cancel producing a comparatively quite supply rail over a broad band. The Master phase uses the falling edge of the SYNC clock to initiate the Master switching cycle with the non-overlap period before the rising edge of LX, while the Slave phase internally inverts the SYNC input and uses the falling edge of the inverted copy to start it's switching cycle. This is independent of whether the Master phase is configured for an external clock (Master M/S = PGND) or its internal clock (Master M/S = VIN). The Master Error Amplifier and Compensation controls the two phase regulator while the Slave Error Amplifier is disabled.

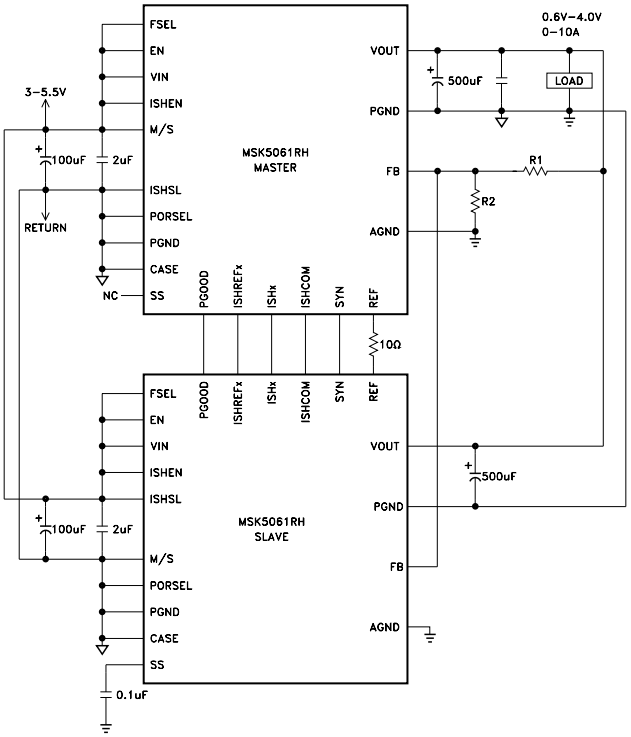
TOTAL DOSE RADIATION TEST PERFORMANCE

Radiation performance curves for TID testing have been generated for all radiation testing performed by TTM Technologies. These curves show performance trends throughout the TID test process and can be located in the MSK5061RH radiation test report. The complete test report is available in the RAD HARD PRODUCTS section of the TTM Technologies website.

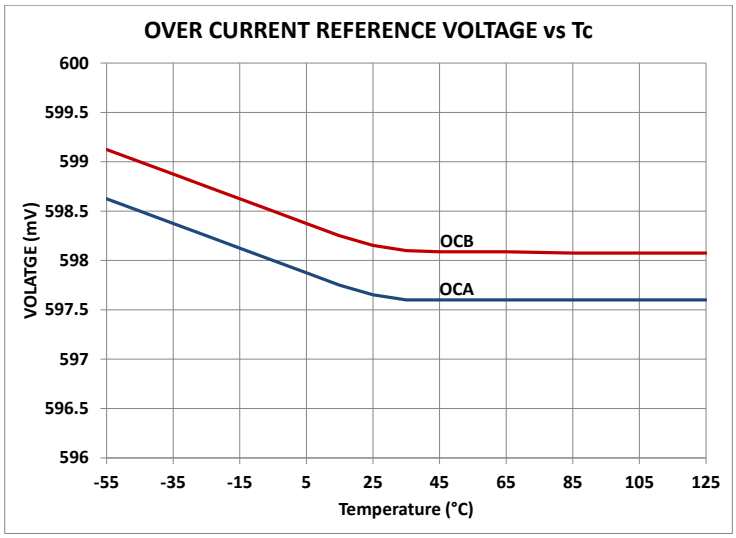
TYPICAL APPLICATION CIRCUIT

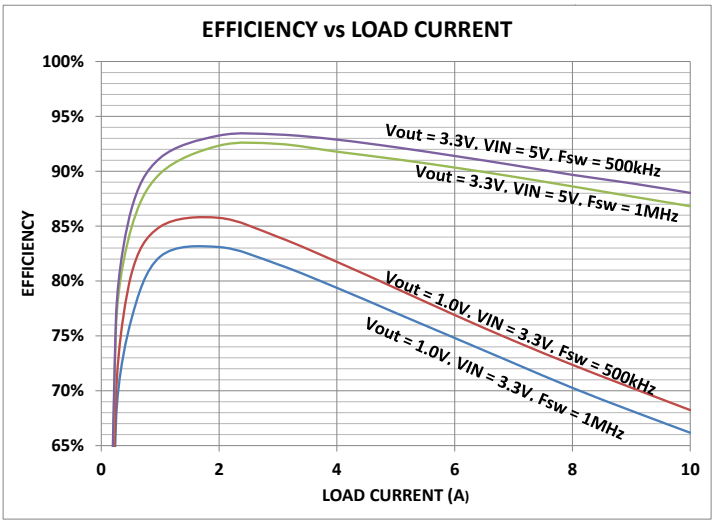


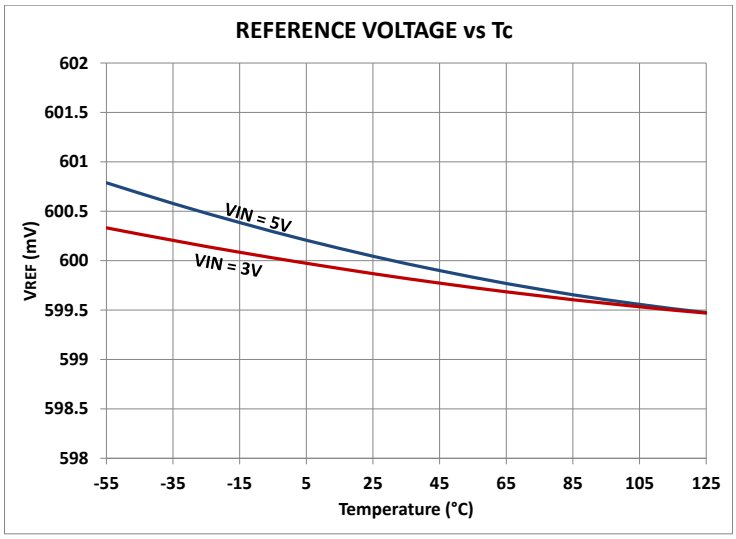
TYPICAL APPLICATION CIRCUIT, CURRENT SHARING

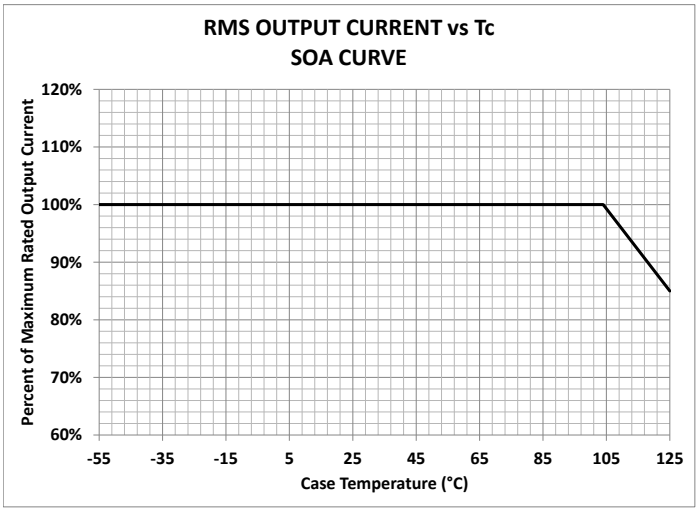


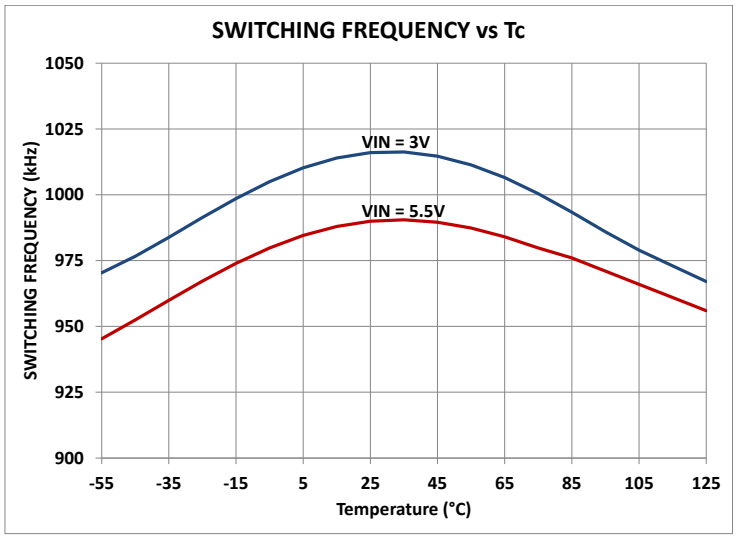
TYPICAL PERFORMANCE CURVES

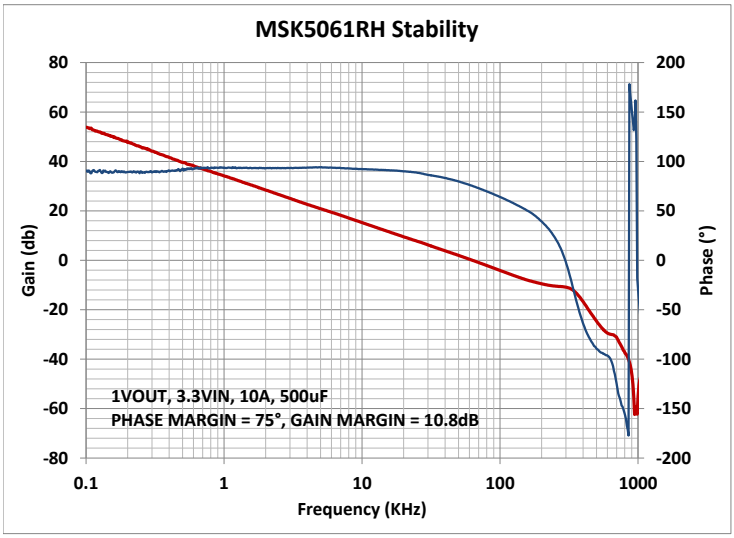




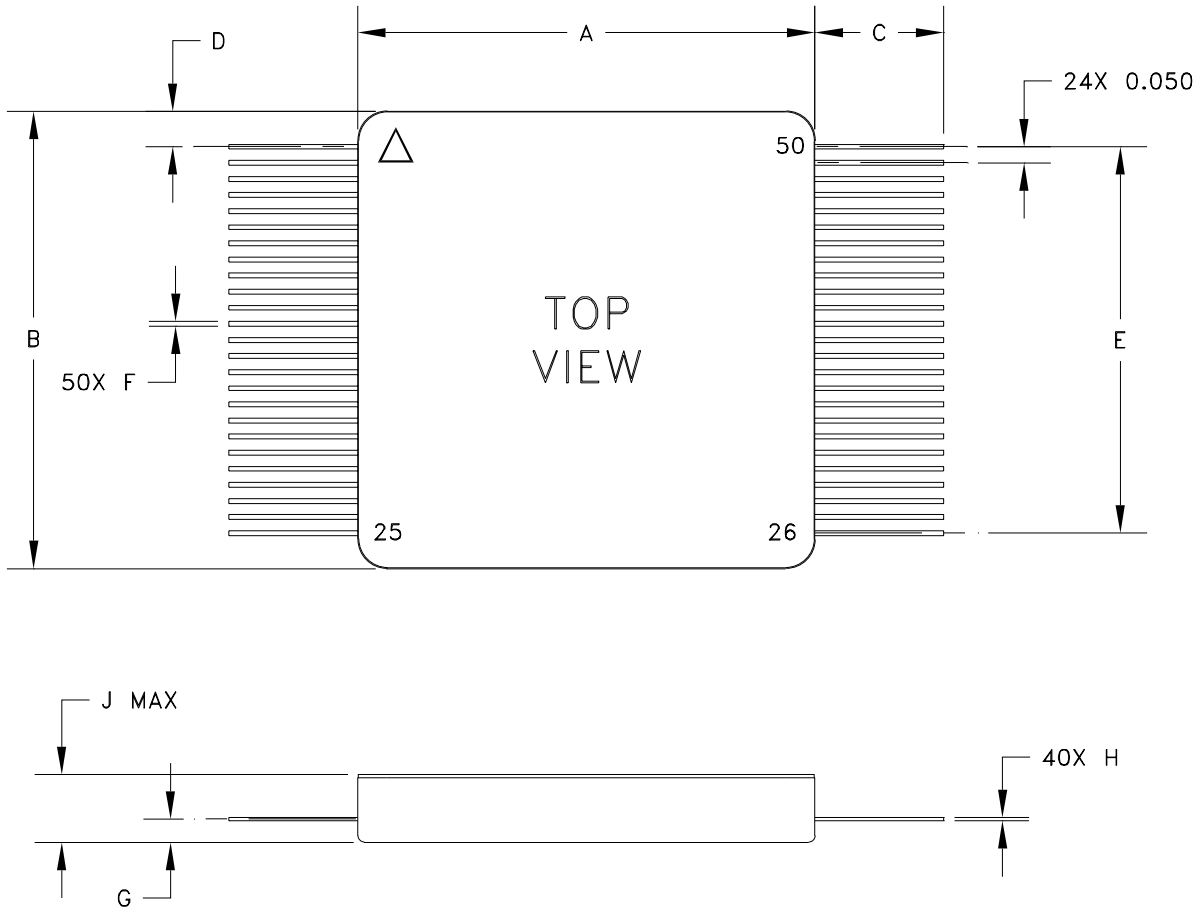








MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	1.410	1.430
B	1.410	1.430
C	0.400	———
D	0.095	0.125
E	1.195	1.205
F	0.012	0.018
G	0.062	0.082
H	0.008	0.012
J	———	0.220

ESD TRIANGLE INDICATES PIN 1
WEIGHT = TBD GRAMS TYPICAL

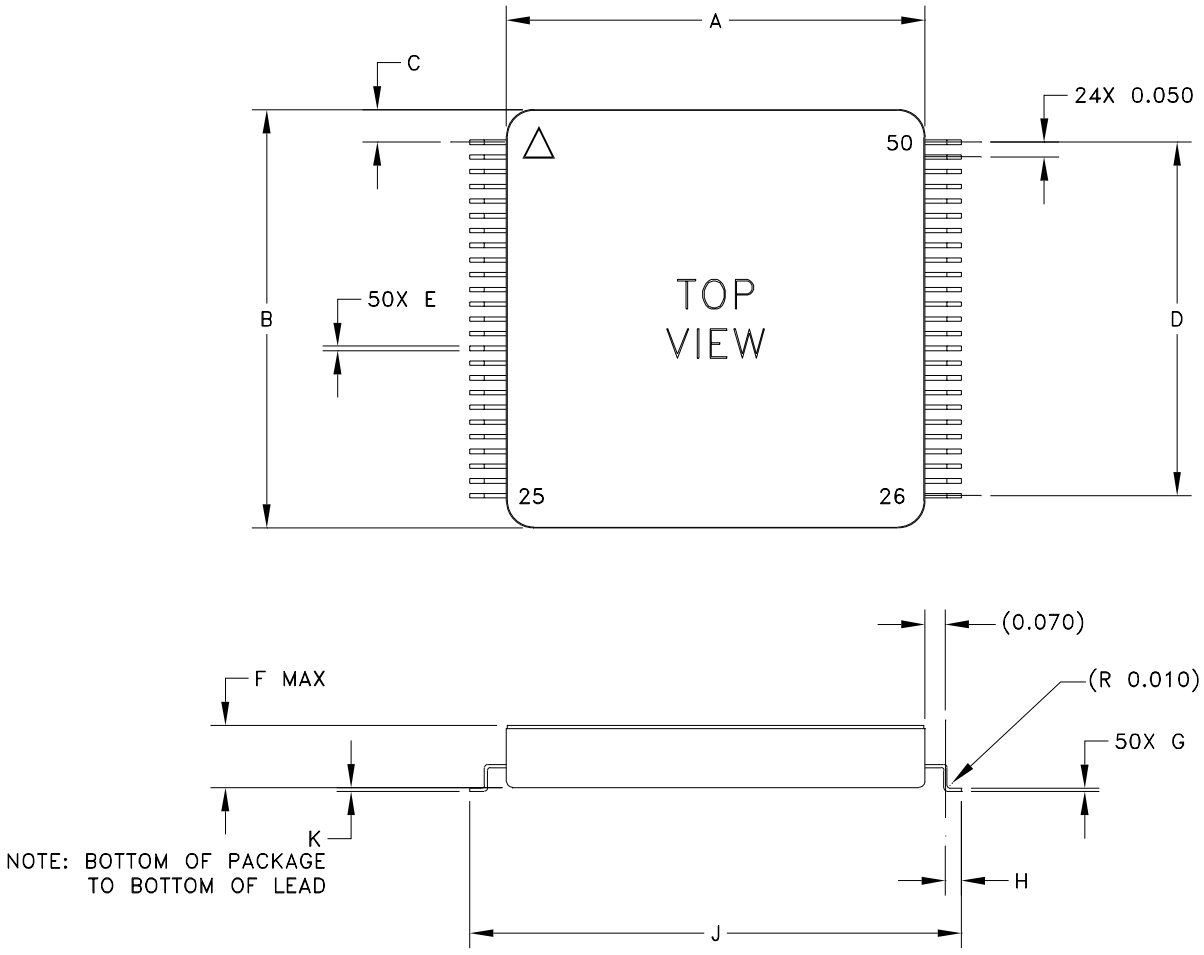
ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5061 H RH —

LEAD FORM OPTION
BLANK = STRAIGHT; G = GULL WING
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
GENERAL PART NUMBER

MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	1.410	1.430
B	1.410	1.430
C	0.095	0.125
D	1.195	1.205
E	0.012	0.018
F	———	0.220
G	0.008	0.012
H	0.045	0.065
J	1.660	1.680
K	0.008	0.018

ESD TRIANGLE INDICATES PIN 1
WEIGHT = TBD GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5061 H RH G

LEAD FORM OPTION
BLANK = STRAIGHT; G = GULL WING
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
A	Released	12/14	Initial Release
B	Released	3/15	Revise package dimensions, equivalent schematic and pin-out
C	Released	6/16	Revise specification limits and performance curves
D	Released	11/16	Change status to Released, update for Radiation Test Completion
E	Released	12/21	Remove MIL-PRF-38535, update company name and website