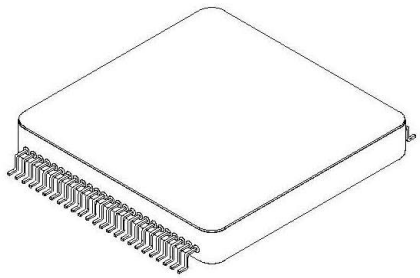
MIL-PRF-38534 CERTIFIED FACILITY

RAD HARD 6A SWITCHING REGULATOR 5062RH

FEATURES:

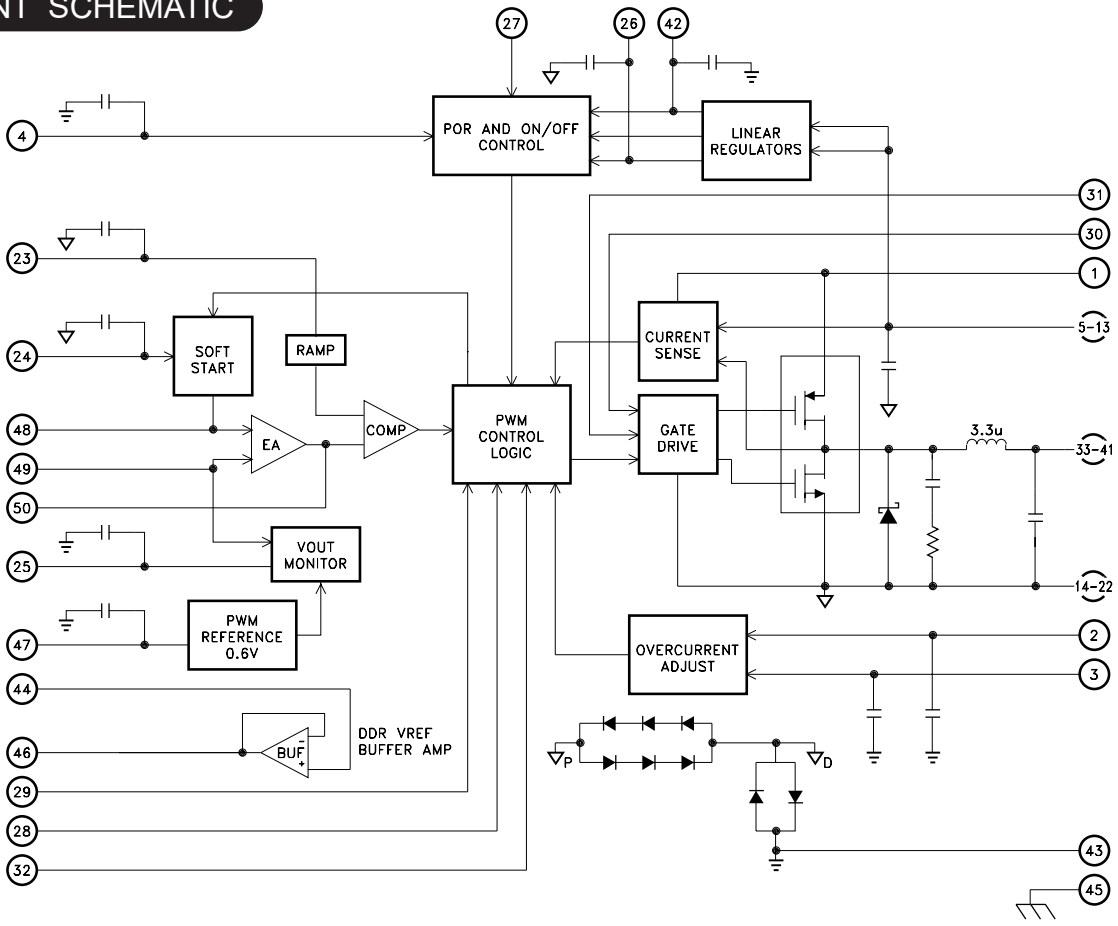
- Total Dose Hardened to 100Krad(Si) (Method 1019.7 Condition A)
- Total Dose tested to 300Krad(Si) (Method 1019.7 Condition A)
- TOR Ready, Designed and Derated to MIL-STD-1547B and NASA EEE-INST-002
- Integrated Inductor
- Adjustable Output +0.6V to ≈ 90% of VIN
- Voltage Mode Control with Feed-Forward
- Buffer Amplifier and Synchronous Switches Support DDR Memory Applications
- 300kHz or 500kHz Fixed Frequency and Synchronizable
- Output Current Monitor Pin
- Externally Adjustable Loop Compensation
- User Selected Scalable Power Switches and Diode Emulation Mode
- Soft-Start, Enable, PGOOD Flag and Power on Reset Feature Simplify Sequencing.
- Contact TTM Technologies for MIL-PRF-38534 Qualification



DESCRIPTION:

The MSK5062RH is a radiation hardened adjustable output switching voltage regulator. The wide input and output range, 6A output current and full complement of features makes this regulator an ideal solution for many space power applications. The integrated inductor and passives reduce design time and board area. All internal components have been designed to satisfy even the most stringent reliability requirements, mitigating program design-in risks. The MSK5062RH is hermetically sealed in a 50 pin flatpack and is available with straight or gullwing leads.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- GEO and LEO satellite system power supply
- Launch vehicle systems
- Microprocessor, FPGA power source
- DDR Memory supply voltages

PIN-OUT INFORMATION

1	IMON	26	VREFD
2	OCSET A	27	ENABLE
3	OCSET B	28	FSEL
4	POR	29	SYNC
5	VIN1	30	SEL1
6	VIN2	31	SEL2
7	VIN3	32	DE
8	VIN4	33	VOUT1
9	VIN5	34	VOUT2
10	VIN6	35	VOUT3
11	VIN7	36	VOUT4
12	VIN8	37	VOUT5
13	VIN9	38	VOUT6
14	PGND1	39	VOUT7
15	PGND2	40	VOUT8
16	PGND3	41	VOUT9
17	PGND4	42	VREFA
18	PGND5	43	AGND
19	PGND6	44	BUFIN+
20	PGND7	45	CASE
21	PGND8	46	BUFOUT
22	PGND9	47	VREF
23	RT	48	NI
24	SS	49	FB
25	PGOOD	50	VERR

ABSOLUTE MAXIMUM RATINGS ⑥

VIN..... 13.7V
VSIGNAL.... ⑧ ..... VREFA + 0.3V
VDIGITAL... ⑨ ..... VREFD + 0.3V
I_{OUT} VOUT Source Current (All Power Blocks)..... 9A
I_{OUT} VOUT Sink Current (All Power Blocks)..... -4A
Case Operating Temperature Range
MSK5062K/H RH..... -55°C to +125°C
MSK5062RH..... -40°C to +85°C
MSK5062EDU.... ⑩ ..... -40°C to +85°C

T_{ST} Storage Temperature Range..... -65°C to +150°C
T_{LD} Lead Temperature Range
(10 Seconds)..... 300°C
T_J Junction Temperature..... 150°C
ESD Rating..... Class 2

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ① ⑦	Group A Subgroup	MSK5062H/K RH			MSK5062RH/EDU			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Current	VIN = 13.2V	1, 2, 3	-	80	125	-	80	125	mA
Standby Supply Current	VIN = 13.2V, SEL1 = SEL2 = 5V	1, 2, 3	-	20	30	-	20	30	mA
Shutdown Supply Current	VIN = 13.2, ENABLE = 0V	1, 2, 3	-	1.5	3	-	1.5	15	mA
VREFA Tolerance	VIN = 13.2V, RLOAD = 110Ω	1, 2, 3	4.5	5	5.5	4.5	5	5.5	V
VREFD Tolerance	VIN = 13.2V, RLOAD = 110Ω	1, 2, 3	4.5	5	5.5	4.5	5	5.5	V
POR Input Voltage		1, 2, 3	0.56	0.6	0.64	0.56	0.6	0.64	V
POR Sink Current	POR = 0.5V	1, 2, 3	9.6	12	14.4	9.6	12	14.4	uA
ENABLE VIH Voltage		1, 2, 3	2	-	-	2	-	-	V
ENABLE VIL Voltage		1, 2, 3	-	-	0.8	-	-	0.8	V
ENABLE Leakage		1, 2, 3	-	1	10	-	1	10	uA
SEL1, SEL2 VIH Voltage ②		1, 2, 3	2	-	-	2	-	-	V
SEL1, SEL2 VIL Voltage ②		1, 2, 3	-	-	0.8	-	-	0.8	V
SEL1, SEL2 Leakage Current	SEL1 = 4.5V, SEL2 = 5V	1, 2, 3	-	1	10	-	1	10	uA
Switching Frequency	FSEL = VREFD	1, 2, 3	255	300	345	255	300	345	kHz
	FSEL = 0V	1, 2, 3	425	500	575	425	500	575	
Minimum on Time ②		1, 2, 3	-	250	-	-	250	-	nS
Minimum off Time ②		1, 2, 3	-	160	-	-	160	-	nS
External Synchronization Frequency Range	FSEL = 5V	1, 2, 3	255	300	345	255	300	345	kHz
	FSEL = 0V	1, 2, 3	425	500	575	425	500	575	
SYNC VIH Voltage		1, 2, 3	2	-	-	2	-	-	V
SYNC VIL Voltage		1, 2, 3	-	-	0.8	-	-	0.8	V
Soft-Start Source Current	SS = 0V	1, 2, 3	20	23	27	20	23	27	uA
PGOOD Sink Current	VIN = 3V, PGOOD = 0.4V, EN = 0V	1, 2, 3	7.2	-	-	7.2	-	-	mA
PGOOD Leakage Current	PGOOD = VIN = 13.2V	1, 2, 3	-	-	1	-	-	1	uA
Reference Voltage Tolerance		1, 2, 3	0.594	0.6	0.606	0.594	0.6	0.606	V
FB Input Leakage Current	VFB = VREF, VIN = 13.2V	1, 2, 3	-	-	250	-	-	250	nA
Buffer Amplifier Offset Voltage		1, 2, 3	-4	0	4	-4	0	4	mV
VOUT Regulation	3V ≤ VIN ≤ 13.2V; 0A ≤ I_{OUT} ≤ 6A; FSEL = VREFD	1, 2, 3	-0.5	-0.05	0.5	-0.5	-0.05	0.5	%
Current Limit	ROCSETA = ROCSETB = 6KΩ 0.1%	1, 2, 3	3.8	5.5	7.2	3.8	5.5	7.2	A
IMON Gain	IIMON/I_{OUT}, I_{OUT} = 6A	1, 2, 3	8.9	10.5	12.2	8.9	10.5	12.2	uA/A
Efficiency	VIN = 12V, VOUT = 5.0V, I_{OUT} = 3A	1, 2, 3	85	90	-	85	90	-	%
Thermal Resistance ②	Junction to case @ 125°C	-	-	2.4	3.8	-	2.4	3.8	°C/W

ELECTRICAL SPECIFICATIONS CONT'D

NOTES:

① Unless otherwise specified VIN = 5V, VOUT = 1.5V, Rload = 2.5KΩ, ENABLE = 5V; FSEL = SEL1 = SEL2 = 0V, ROCSETA = ROCSETB = 5KΩ

② Guaranteed by design but not tested. Typical parameters are representative of device performance but are for reference only.

③ Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise specified.

④ Military grade “H” and “K” suffix devices shall be 100% tested to subgroups 1, 2, 3, 4, 5 and 6.

⑤ Subgroup 1,4 TC = +25°C
Subgroup 2,5 TC = +125°C
Subgroup 3,6 TC = -55°C

⑥ Continuous operation at or above the absolute maximum ratings may adversely affect the device performance and/or life cycle.

⑦ Pre and post irradiation limits, up to 100Krad(Si) TID, are identical unless otherwise specified.

⑧ Signal Pins; POR, FB, NI, VERR, OCSETA, OCSETB, BUFOUT, BUFIN+, IMON and REF pins.

⑨ Digital Control Pins; FSEL, EN, SYNC, SEL1, SEL2 and DE pins.

⑩ MSK5062EDU does not use RAD Hard Die, Post irradiation performance is not guaranteed.

APPLICATION NOTES

PIN FUNCTIONS

IMON – IMON is a current source output that is proportional to the sensed current through the regulator. If not used it is recommended to tie IMON to VREFA. It is also acceptable to tie IMON to GND through a resistor.

OCSETA, OCSETB – Connect a resistor from each of these pins to the AGND plane to set the output current limit threshold. See the Current Limit section for more details.

POR – The POR pin is the power-on reset input to the IC. This is a comparator-type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC.

VINx – The VIN pins are the input supply pins for all internal circuitry. High di/dt switching currents are conducted through these pins. Locally decouple VIN to PGND with a mix high frequency ceramic capacitors and low ESR tantalum. Provide sufficient bulk capacitance to ensure a low impedance bus and minimize input voltage ripple.

PGNDx – The PGND pins connect to the internal power ground plane. High di/dt switching currents are conducted through these pins. Provide a continuous low impedance ground path between the MSK5062RH PGND, the input supply return, and the load. Avoid layouts that force load return current to cross the AGND reference path.

RT – Connect a resistor between VIN and RT to provide voltage feed-forward to keep a constant modulator gain as VIN varies. While operating at 500KHz a 22kΩ RT resistor sets the modulator gain at 5 nominal. While operating at 300KHz a 36kΩ RT resistor sets the modulator gain at 4.8 nominal.

SS – The Soft Start pin provides control of turn on surge currents. A 23µA current source charges the internal SS capacitor and sets the output ramp time to approximately 2.6mS. Connect additional capacitance to reduce the output ramp rate. Further application guidance is provided in the Start Up Considerations section.

PGOOD – The PGOOD pin is an open-drain logic output that is pulled to PGND when the output voltage is outside a ±11% typical regulation window. This pin can be pulled up to any voltage from 0V to 13.2V, independent of the supply voltage. A 1kΩ to 10kΩ pull-up resistor is recommended.

VREFD – The VREFD pin is the output of an internal linear regulator and the bias supply input to the internal digital control circuitry.

ENABLE – The ENABLE pin is a logic-level enable input. Pulling this pin low powers down the device, placing it into a very low power sleep mode.

FSEL – The FSEL pin is the oscillator frequency select input. Tie this pin to 5V to select a 300kHz nominal oscillator frequency. Tie this pin to the PCB ground plane to select a 500kHz nominal oscillator frequency.

SYNC – The SYNC pin is the frequency synchronization input to the IC. Tie this pin to GND to free-run from the internal oscillator or connect it to an external clock for external frequency synchronization.

SEL1, SEL2 – The SEL1 and SEL2 pins form a 2-bit logic input that set the number of active power blocks. This allows the MSK5062RH current capability to be tailored to the application and achieve the highest possible efficiency.

DE – The DE pin is a logic level input that enables or disables Diode Emulation. When it is HIGH, diode emulation is enabled and the inductor current is allowed to go discontinuous.

VOUTx – The VOUT pins are connected to the internal output inductor. Connect VOUT as close as possible to the load to minimize bus impedance. Connecting 500 to 1000µF low ESR bulk capacitance to VOUT is typically sufficient to ensure good transient response. Some ceramic capacitance near the load is typically required to support fast load transients. A mix of high frequency ceramic capacitors and low ESR tantalum are recommended. See Output Capacitor Selection paragraph.

VREFA – The VREFA pin is the output of an internal linear regulator and the bias supply input to the internal analog control circuitry.

AGND – The AGND pin provides a low noise signal reference for the internal control circuitry. For optimum regulation performance, connect AGND and PGND together near the ground side of the load.

BUFIN+ The BUFIN+ pin is the input to the internal unity gain buffer amplifier. For DDR memory power applications, connect the VTT voltage to this pin.

CASE – The CASE pin is electrically connected to the case.

BUFOUT - The BUFOUT pin is the output of the buffer amplifier. In DDR power applications, connect this pin to the reference input of the DDR memory. The buffer needs a minimum of 1.0µF load capacitor for stability.

VREF - The VREF pin is the output of the 0.6V internal reference. This pin is connected to NI-. This pin must not be otherwise loaded.

NI - The NI pin is the non-inverting input to the internal error amplifier. Connect this pin to the REF pin for typical applications or to the VDDQ rail through a divider for DDR memory VTT power applications.

PIN FUNCTIONS

FB – The FB pin is the inverting input to the internal error amplifier. An external type III compensation network should be connected between this pin and the VERR pin. The connection between the FB resistor divider and the load should be a low impedance Kelvin connection to optimize performance.

VERR – The VERR pin is the output of the internal error amplifier. An external compensation network should be connected between this pin and the FB pin.

INPUT POWER SUPPLY BYPASSING

Current is drawn from the input bus in roughly trapezoidal pulses with very fast edge rates, and consequently consists of a broad frequency spectrum. High quality low ESR/ESL ceramic capacitors connected directly across the VIN and PGND pins are recommended to provide a low impedance to the high frequency components of the wave form confining them local to the regulator, thereby limiting conducted EMI. Minimizing the area of the VIN-CIN-PGND loop will help minimize radiated EMI. The MSK5062RH simplifies application with the inclusion of significant internal ceramic capacitance. The internal and external input capacitors source the AC component of the switched current into the regulator. The RMS ripple current seen by the input capacitors is high, approaching a maximum of 0.5 x Iout at approximately 50% duty cycle. Sufficient bulk capacitance must be provided to minimize ripple voltage seen by the device and ensure stable operation. As a general rule of thumb, VIN ripple should be less than 3 to 5% of VIN. Selection of the bulk input capacitors will likely involve a parallel combination of several tantalum and ceramics to allow proper voltage and ripple current derating. Satisfying those requirements will almost invariably result in sufficient bulk to minimize ripple voltage and ensure stable operation.

OUTPUT CAPACITOR SELECTION

450uF of low ESR tantalum capacitance mounted near the MSK5062RH and properly designed compensation has been shown to provide good stability margins and dynamic response. The bulk output capacitance parasitic ESR and ESL, the non-zero impedance between the regulator output and the load terminals, and finite bandwidth will cause a transient voltage signal to develop in proportion to the magnitude of the load step. Additional low ESR ceramic capacitance mounted near the load can help mitigate the transient voltage excursions. Care should be exercised in capacitor selection such that the loop maintains adequate stability margin.

OUTPUT VOLTAGES SELECTION

The output voltage is governed by the following equation:

$$V_{OUT} = VREF \times \left(1 + \frac{R1}{R2}\right)$$

Resistors in the 1KΩ to 5KΩ range are typically used to minimize power and leakage current effects. Some loop compensation can be achieved by placing R –C networks in parallel with either R1 and/or R2. Any compensation efforts should be verified by analysis and measurement.

ENABLE

When the voltage on the ENABLE pin exceeds its logic rising threshold, the controller monitors the POR voltage before initiating the soft-start function for the PWM regulator. When ENABLE is pulled low, the device enters shutdown mode and the supply current drops to a typical value of 1.5mA. All internal power devices are held in a high impedance state while in shutdown mode. Due to the internal 5V clamp, the ENABLE pin should be driven no higher than 5V or excessive leakage current may be seen on the pin. In standalone applications the ENABLE pin may be tied to an input voltage >5V through a 50kΩ resistor to minimize the current into the ENABLE pin. The current should not be allowed to exceed 160µA at any operating voltage.

POWER ON RESET

After the ENABLE input requirements are met, the MSK5062RH remains in shutdown until the voltage at the POR pin rises above its threshold. The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the VIN pins. The POR circuit features a comparator type input. The POR circuit allows the level of the input voltage to precisely gate the turn-on/turn-off of the regulator. An internal current sink with a typical value of 12µA is only active when the voltage on the POR pin is below the enable threshold so it can pull the POR pin low. VIN POR thresholds can be selected according to the following equations.

$$\text{VIN Rising Threshold} = V_{REF} \times \left(1 + \frac{R3}{R4}\right) + R3 \times I_{POR}$$

$$\text{VIN Falling Threshold} = V_{REF} \times \left(1 + \frac{R3}{R4}\right)$$

SOFT START

Once the POR and ENABLE thresholds have been satisfied, a soft start cycle will be initiated. The Soft Start circuit limits the surge current drawn to charge the output capacitors by controlling the ramp rate of the output voltage. This feature can also be exploited to implement coincident and ratiometric tracking supplies required by many cutting edge digital systems. During start up the error amplifier reference voltage is clamped to the SS pin while a 23µA current source charges the SS pin capacitor. The soft start ramp time can be adjusted over a range of 2.6ms to 214ms. Determine the desired ramp rate and use the following equation to select the corresponding soft start capacitor.

$$C_{SSEXT} = \frac{T_{SS} \times I_{SS}}{V_{REF}} - 0.1uF$$

Once the SS pin reaches the reference voltage and the output voltage is within ≈ 90% of the set point, the PGOOD pin will transition to the high state. The soft-start capacitor is immediately discharged by a 3.0Ω resistor whenever POR conditions are not met or ENABLE is pulled low. The soft-start discharge time is equal to 256 clock cycles.

POWER GOOD

A power-good indicator is the final step of initialization. After a successful soft-start, the PGOOD pin releases and the voltage rises with an external pull-up resistor. The PGOOD signal transitions low immediately when the ENABLE pin is pulled low. The PGOOD pin is an open-drain logic output and can be pulled up to any voltage from 0V to 13.2V. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ.

SYNCHRONIZATION

The MSK5062RH, can be synchronized to an external clock with a frequency range of 500kHz ±15% or 300kHz ±15%, depending on the state of the FSEL pin. The SYNC pin accepts the external clock signal and the regulator will be synchronized in phase with the external clock. During start-up the regulator will use its internal oscillator to regulate the output voltage. Once soft-start is complete and PGOOD is released, the regulator will synchronize to the external clock signal. This feature allows the MSK5062RH

regulator to be the power source to the external components that will be providing the external clock without the requirement that a signal must be present at the SYNC pin before start-up.

DISABLING POWER BLOCKS

SEL1 and SEL2, form a 2-bit logic input that are used to turn off the internal power blocks. Depending on the state of the SEL1 and SEL2 pins, the MSK5062RH can operate with 2, 4 or 10 power blocks on or have all the outputs in a tri-state mode. This allows the designer to reduce switching losses in low current applications, where all power blocks are not needed to supply the load current.

SEL2	SEL2	ACTIVE POWER BLOCKS	LOAD CAPABILITY T_J = 125°C
0	0	10	9A
0	1	4	3.6A
1	0	2	1.8A
1	1	NONE	NA

CURRENT LIMIT

The overcurrent threshold is based on the resistor value tied from pins OCSETA and OCSETB to AGND. Upon detection of an overcurrent condition, the upper MOSFETs will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will increment. However, if the sampled current falls below the threshold the counter is reset. If there are 4 sequential OC fault detections, the counter will overflow and the regulator will be shut down under an overcurrent fault condition, pulling PGOOD low.

After the regulator shuts down, it enters a delay interval, allowing the device to cool. The delay interval is approximately equal to 512 clock cycles plus 1 soft-start interval. The overcurrent counter is reset entering the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft starts, the power-good signal goes high and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shutdowns the output again. This hiccup mode continues indefinitely until the output soft starts successfully.

The following equation determines the OCSETA and OCSETB resistors for a given peak current limit threshold based on the N number of active power blocks.

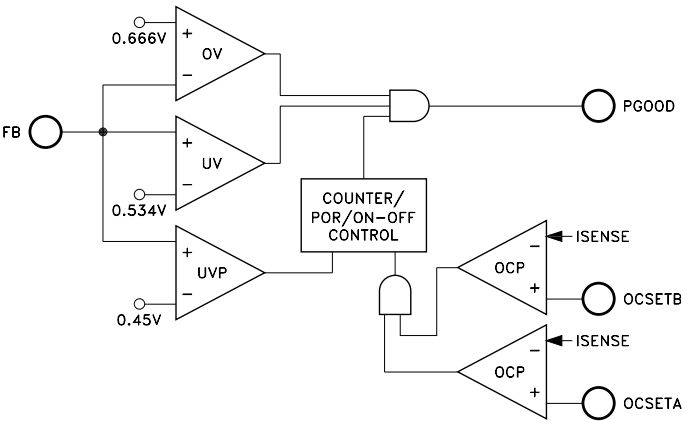
$$R_{OCSETA/B} = \frac{3602.4 \times N}{\text{Peak Current Threshold (A)}}$$

UNDERVOLTAGE AND OVERVOLTAGE MONITOR

The PGOOD pin is an open-drain logic output which indicates that the converter is operating properly and the output voltage is within a set window. The Undervoltage (UV) and Overvoltage (OV) comparators create the output voltage window. The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds. If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage within the power-good window.

UNDERVOLTAGE PROTECTION

A hysteretic comparator monitors the FB pin. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage, typically 75%. Once the comparator trips, indicating a valid undervoltage condition, an undervoltage counter increments. The counter is reset if the feedback voltage rises back above the undervoltage threshold plus hysteresis typically 3.5% of VREF. If there are 4 consecutive undervoltage detections the counter will overflow and the undervoltage protection logic shuts down the regulator, pulling PGOOD low. After the regulator shuts down, it enters a delay interval, approximately equivalent to 512 clock cycles plus 1 soft-start interval, allowing the device to cool. The undervoltage counter is reset entering the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft starts, the power-good signal goes high and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This hiccup mode continues indefinitely until the output soft starts successfully. The following diagram illustrates the functional relationship of the protection features and PGOOD pin state.



IMON, CURRENT SENSE OUTPUT

The IMON pin outputs a high speed analog current that is proportional to the sensed peak current through the active power blocks. In typical applications, a resistor RIMON is connected to the IMON pin to convert the sensed current to voltage, VIMON, which is proportional to the peak current. Where N is the number of active power blocks:

$$V_{IMON} = 100 \times 10^{-6} \times \frac{I_{SAMPLE} \times R_{IMON}}{N}$$

ISAMPLE is a function of the RMS load current IOUT, the inductor ripple current ΔIL, the sampling time t (typically 225ns), the switching frequency FSW, and duty cycle D.

$$I_{SAMPLE} = I_{OUT} + \frac{\Delta IL}{2} - \left(\Delta IL \frac{Ts \times Fsw}{(1 - D)}\right)$$

If the IMON pin is not used, connect to VREFA or through a resistor to ground. A low value capacitor should be connected from IMON to AGND to mitigate SEE transients and noise.

DIODE EMULATION

Pulling the DE pin high enables diode emulation mode and allows for higher efficiency at low load current. In DE mode the lower MOSFETS are turned off when the inductor current crosses zero preventing unnecessary power loss. Since diode emulation prevents the low-side MOSFET from sinking current, no negative spike at the output is generated during prebiased startup when DE mode is active. After a significantly fast load release transient, diode emulation will not allow the converter to bring the output voltage back down following the hump created by the inductor energy dump into the output capacitor bank.

The MSK5062RH overcomes this issue by monitoring the output of the error amplifier and allowing the low-side MOSFET to turn on and sink the necessary current needed to properly regulate the output voltage. The same mechanism allows the converter to properly regulate the output voltage when starting into a prebiased condition where the prebias level is greater than the desired output voltage.

The DE pin is not intended to actively change states while the regulator is operating. If any part of the inductor current is below zero and the DE pin changes state there will be a glitch on the output voltage. However, if the state of the DE pin changes when the inductor current is positive, no change in the operation of the regulator will be seen.

TOTAL DOSE RADIATION TEST PERFORMANCE

Radiation performance curves for TID testing has been generated for all radiation testing performed by TTM Technologies. These curves show performance trends throughout the TID test process and can be located in the MSK5062RH radiation test report. The complete test reports are available in the RAD HARD PRODUCTS section of the TTM Technologies website.

DDR MEMORY APPLICATION

Three tracking voltages are required for DDR memory modules; VDDQ, VTT, and Vref. The unique requirements of the VTT supply is that is must closely track VDDQ and adequately regulate while either sourcing to or sinking current from the VTT rail. Two MSK5062RH can be configured to meet this challenge.

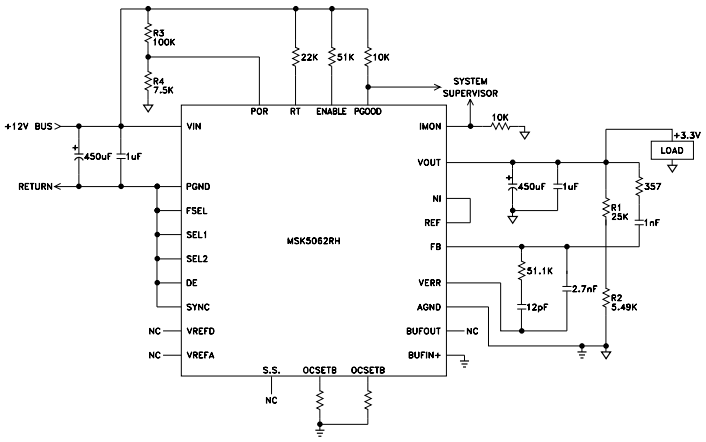
Both VDDQ and VTT are derived independently from the main power source. The first regulator supplies the 2.5V for the VDDQ voltage. The output voltage is set by external dividers RT1 and RB1. The second regulator generates the VTT rail typically = VDDQ/2. The resistor divider network RT2 and RB2 are used to set the output voltage to 1.25V. The VDDQ rail has an additional voltage divider network consisting of RT3 and RB3, the midpoint is connected to the non-inverting input pin of the VTT regulator's error amplifier (NI), effectively providing a tracking function for the VTT voltage. BUFIN+, The non-inverting input of the buffer amplifier is connected to the center point of the external divider from the VDDQ output. The buffer output voltage serves as a 1.25V reference (VREF) for the DDR memory devices. Sourcing capability of the buffer amplifier is 10mA typical (20mA max) and needs a minimum of 1µF load capacitance for stability.

Diode emulation mode of operation must be disabled on the VTT regulator to allow sinking capability. In the event both channels are enabled simultaneously, the soft-start capacitor on the VDDQ regulator should be two to three times larger than the soft-start capacitor on the VTT regulator. This allows the VDDQ regulator voltage to be the lowest input into the error amplifier of the VTT regulator and dominate the
soft-start ramp. However, if the VTT regulator is enabled later than the VDDQ, the soft-start capacitor can be any value based on design goals.

Each regulator has its own fault protections and must be individually configured. All the sink current on the VTT regulator is provided by the VDDQ rail, the overcurrent protection on the VDDQ rail will limit the amount of current that the VTT rail will sink.

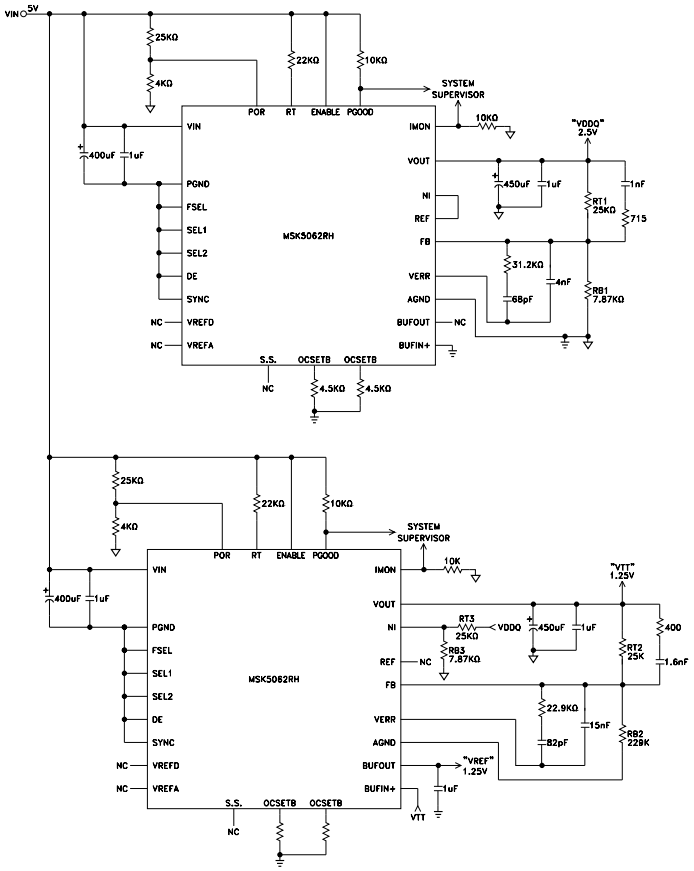
SEL1 and SEL2 may be tied together and used to place the VTT regulator in sleep mode, common to DDR applications. The outputs will be tri-stated, however the buffer amplifier is still active and the VREF voltage will be present even if the VTT is in sleep mode. When SEL1 and SEL2 are asserted low, the VTT regulator will ramp-up the voltage. The ramp is controlled and timing is based on soft-start capacitor value.

TYPICAL APPLICATION CIRCUIT



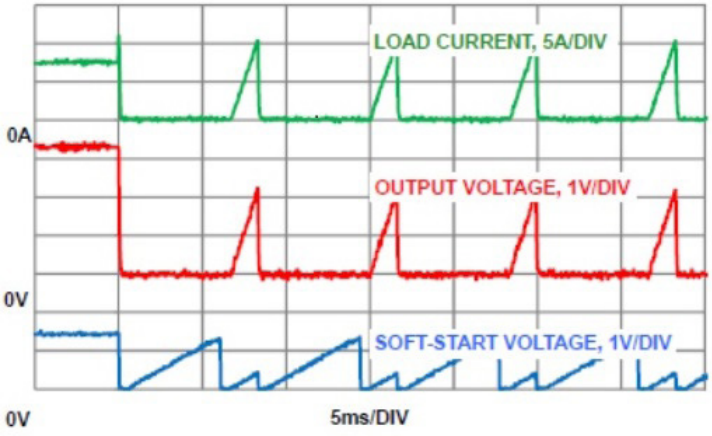
APPLICATION NOTES CONT'D

TYPICAL APPLICATION CIRCUIT, DDR POWER

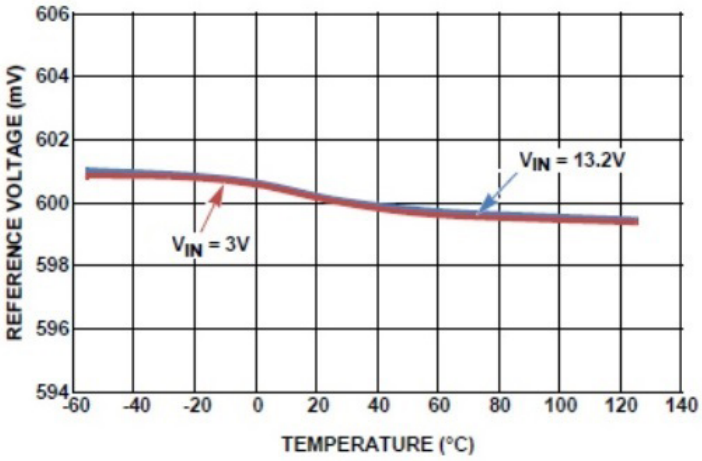


TYPICAL PERFORMANCE CURVES

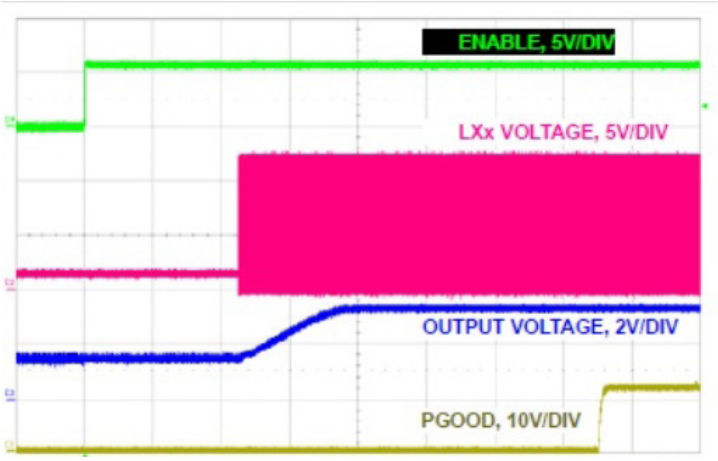
OVERCURRENT BEHAVIOR IN HICCUP MODE



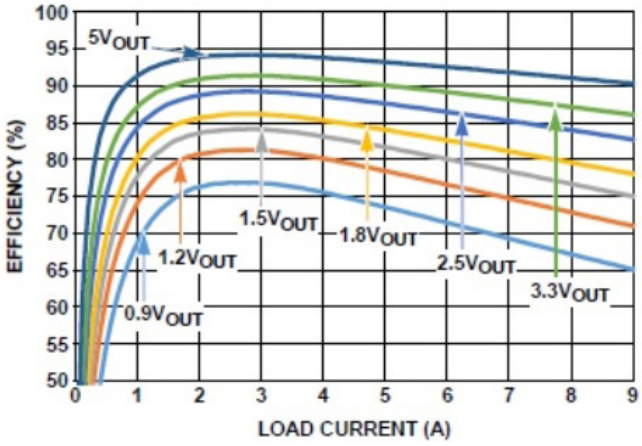
REFERENCE VOLTAGE vs TEMPERATURE



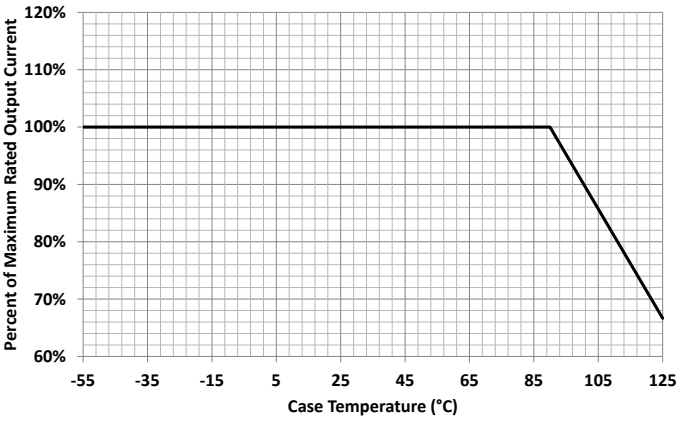
MONOTONIC SOFT-START WITH 1.5V PREBIASED LOAD



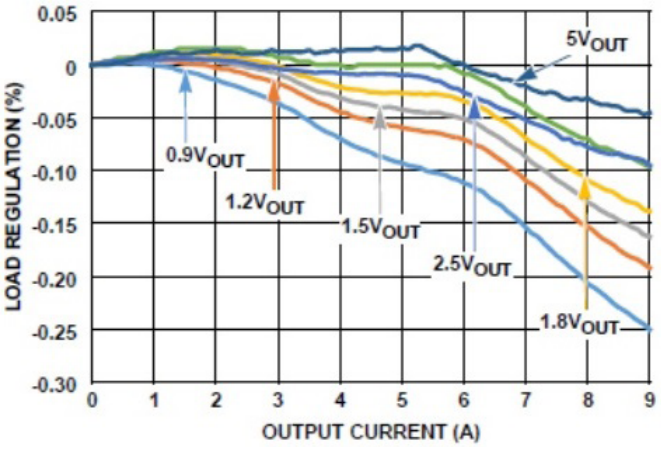
EFFICIENCY vs LOAD, VIN=8V, 300kHz



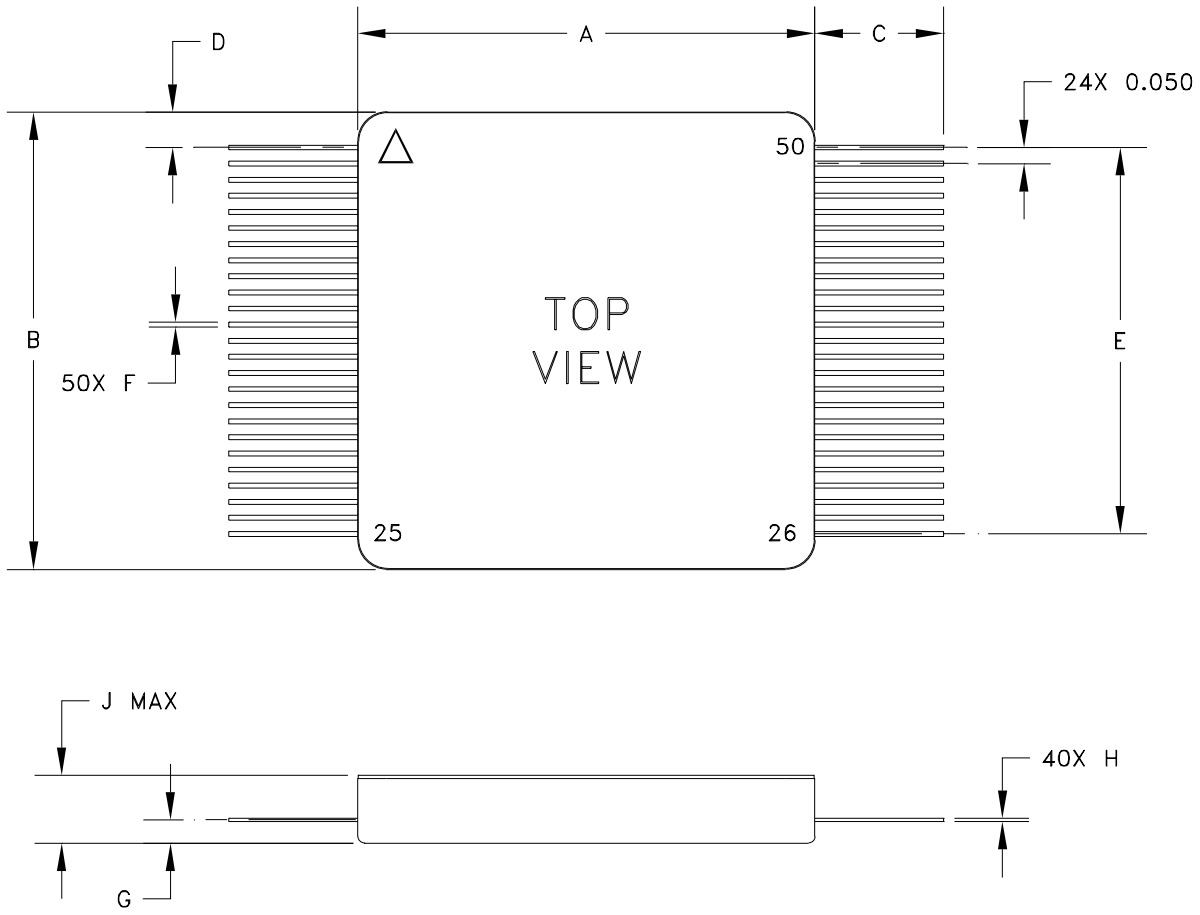
RMS OUTPUT CURRENT vs Tc
SOA CURVE



LOAD REGULATION vs VOUT,VIN=12V



MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	1.410	1.430
B	1.410	1.430
C	0.400	———
D	0.095	0.125
E	1.195	1.205
F	0.012	0.018
G	0.062	0.082
H	0.008	0.012
J	———	0.220

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 20 GRAMS TYPICAL

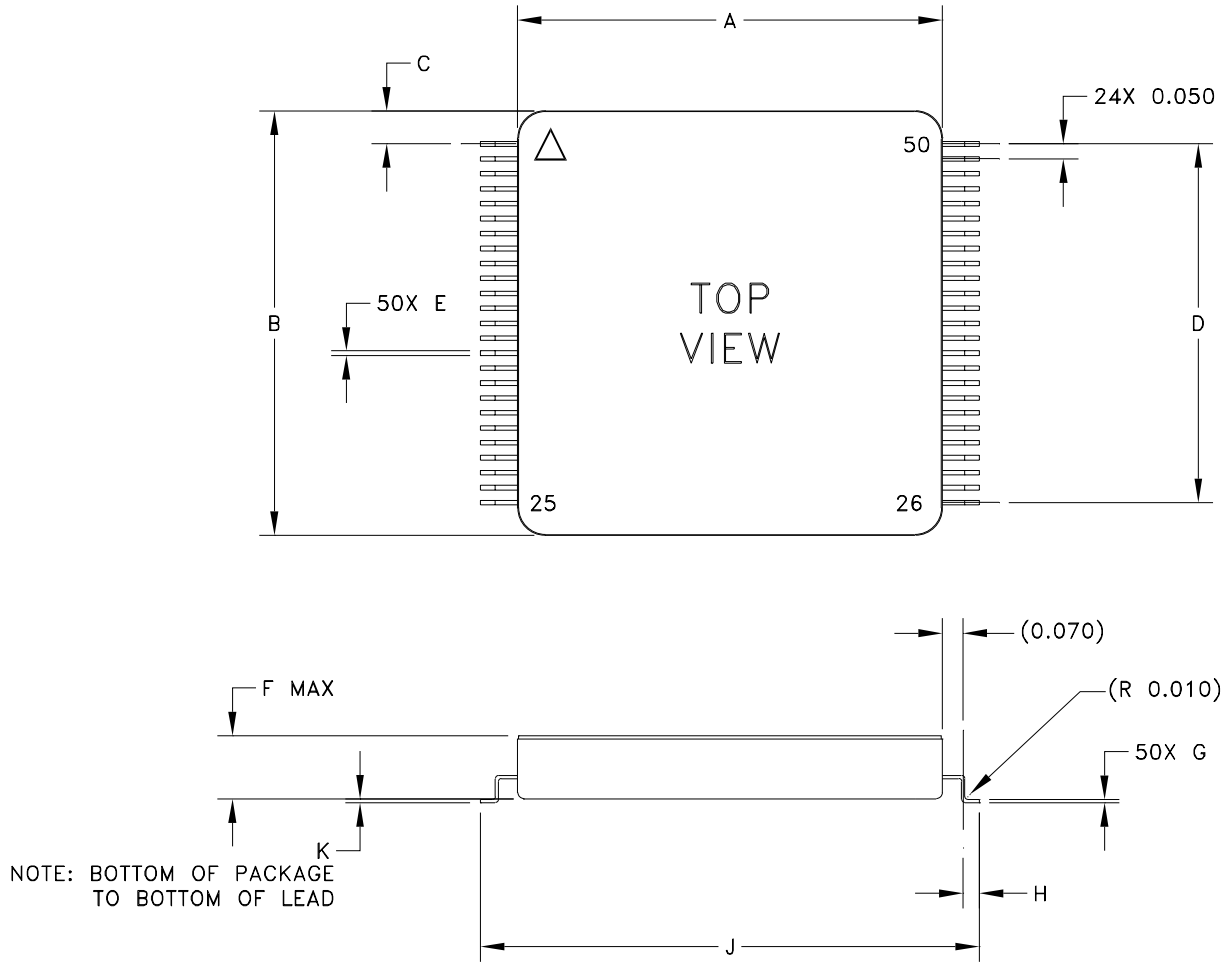
ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5062 H RH

LEAD FORM OPTION
BLANK = STRAIGHT; G = GULL WING
RADIATION HARDENED
SCREENING
EDU = NON-RAD HARD ENG UNITS
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
GENERAL PART NUMBER

MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	1.410	1.430
B	1.410	1.430
C	0.095	0.125
D	1.195	1.205
E	0.012	0.018
F	———	0.220
G	0.008	0.012
H	0.045	0.065
J	1.660	1.680
K	0.008	0.018

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 20 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5062 H RH G

LEAD FORM OPTION
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GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
A	Preliminary	09/16	Initial Release
B	Preliminary	02/17	Add EDU version
C	Released	03/18	Update Radiation Status
D	Released	03/22	Remove MIL-PRF-38535, update company name and website