MIL-PRF-38534 CERTIFIED FACILITY

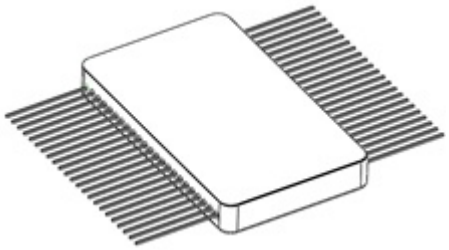
TTM Technologies

RAD HARD HIGH VOLTAGE SYNCHRONOUS SWITCHING REGULATOR

5063RH

FEATURES:

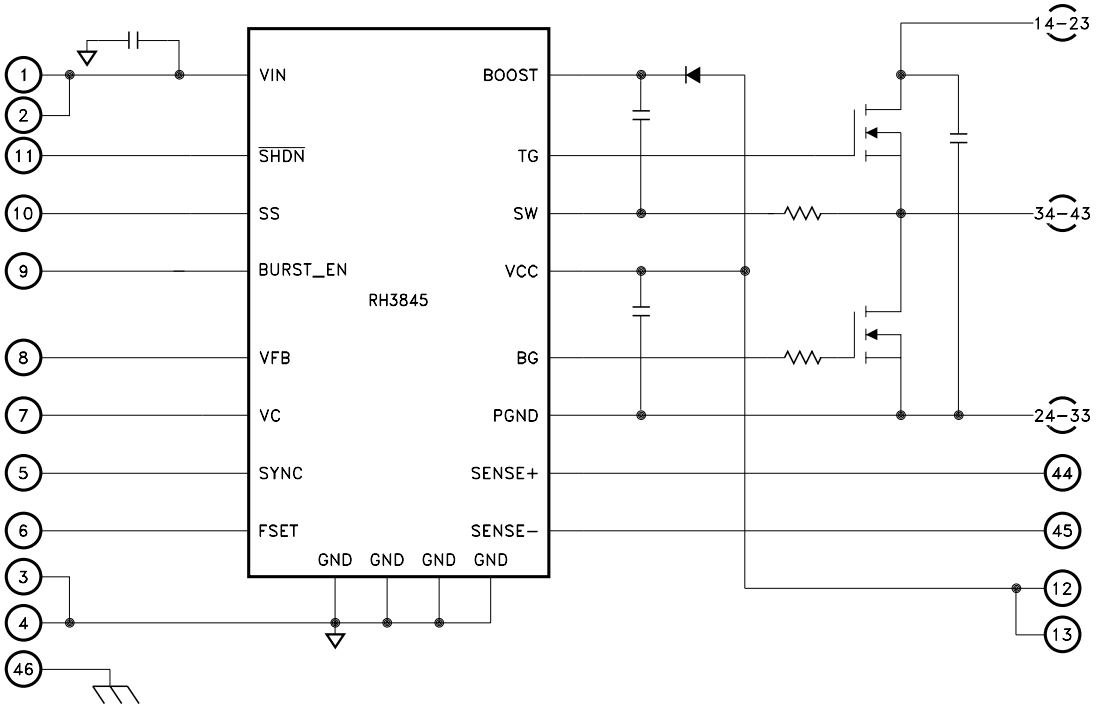
- Manufactured using LINEAR TECHNOLOGY Space Qualified RH3845 Dice
- Radiation Hardened to 300 Krad(Si) (Method 1019.7 Condition A)
- High Voltage Operation: Up to 60V Input, and 36V Output
- Programmable Frequency 100-500KHz, or Synchronizable to 600KHz
- 65µA Shutdown Supply Current
- Antislope Compensation – Current Limit Unaffected by Duty Cycle
- Reverse Inductor Current Inhibit – Improves Efficiency with Light Loads
- External Compensation
- Contact TTM Technologies for MIL-PRF-38534 Qualification Status



DESCRIPTION:

The MSK5063RH is a radiation hardened wide input voltage range step-down synchronous switching regulator. The wide input range, programmable output voltage and switching frequency, make these regulators suitable for a wide variety of medium to high power applications. The adjustable operating frequency provides the flexibility to keep the switching noise out of sensitive frequency bands, and when synchronized, can be ganged out of phase with other regulators for reduced noise and component size. The MSK5063RH is hermetically sealed in a 46 pin flatpack, and is available with straight or gull wing leads.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- POL Applications
- Intermediate Bus Converter
- Satellite System Power Supply
- Step Down Synchronous Regulator
- High Efficiency Subsystem Supply

PIN-OUT INFORMATION

1, 2	VIN	9	MODE	34 - 43	SWOUT
3, 4	SGND	10	SS	44	SENSE+
5	SYNC	11	SHDN	45	SENSE-
6	FSET	12, 13	BIAS	46	CASE
7	COMP	14 - 23	PVIN		
8	VFB	24 - 33	PGND		

CASE = ISOLATED

ABSOLUTE MAXIMUM RATINGS ⑧

VIN	Input Voltage	65V
PVIN	Power Input Voltage	60V
BIAS	Bias Supply Voltage	14V
SWOUT	SWOUT Voltage ⑦	60V to -2V
I_{OUT}	Output Current	10A
V_{SENSE}	SENSE+ and SENSE- Voltages	40V
	Differential Sense Voltage	±1V
	SYNC, COMP, VFB, SS and $\overline{SHDN}$	5V
	MODE	24V
	$\overline{SHDN}$ Pin Currents	1mA
T_{LD}	Lead Temperature Range (10 Seconds)	300°C
T_{ST}	Storage Temperature	-65°C to 150°C
T_J	Junction Temperature	150°C
T_C	Operating Case Temperature	-55°C to +125°C
	ESD Rating	1C

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ① ⑨		Group A Subgroup	MSK5055K/H RH Min.	MSK5055K/H RH Typ.	MSK5055K/H RH Max.	MSK5055RH Min.	MSK5055RH Typ.	MSK5055RH Max.	Units
VIN Min Start Voltage	BIAS OPEN		1, 2, 3	-	-	7.5	-	-	7.5	V
VIN UVLO Threshold (Falling)			1, 2, 3	3.6	3.8	4	3.6	3.8	4	V
		Post 100 Krad(Si)	1	3.55	3.6	4	3.55	3.6	4	V
		Post 300 Krad(Si)	1	3.45	3.5	4	3.45	3.5	4	V
VIN Supply Current ②	BIAS ≥ 9V		1	-	130	-	-	130	-	uA
VIN Shutdown Current ②	$V_{\overline{SHDN}}$ = 0V		1, 2, 3	-	65	-	-	65	-	uA
BIAS Supply Current ②		F_{SYNC} = 100KHz	1	-	16	-	-	16	-	mA
		F_{SYNC} = 600KHz	1	-	63	-	-	63	-	mA
BIAS Current Limit			1, 2, 3	40	-	-	40	-	-	mA
Static Drain-to-Source on Resistance	I_D = 1.0A		1, 2, 3	-	0.06	0.1	-	0.06	0.1	Ohm
Error Amp Reference Voltage	COMP = VFB		1, 2, 3	1.214	1.231	1.250	1.214	1.231	1.250	V
		Post 100 Krad(Si)	1	1.200	1.222	1.250	1.200	1.222	1.250	V
		Post 300 Krad(Si)	1	1.173	1.197	1.250	1.173	1.197	1.250	V
VFB Pin Input Current ②	VFB = V_{REF}		1	-	35	-	-	35	-	nA
$\overline{SHDN}$ Enable Threshold (Rising)			1, 2, 3	1.3	1.37	1.5	1.3	1.37	1.5	V
		Post 300 Krad(Si)	1	1.25	1.3	1.5	1.25	1.3	1.5	V
$\overline{SHDN}$ Threshold Hysteresis ②			1	-	125	-	-	125	-	mA
Current Limit Sense Voltage	(V_{SENSE}+) - (V_{SENSE}-), VFB = 0V		1, 2, 3	85	100	125	85	100	125	mV
		Post 100 Krad(Si)	1	80	103	125	80	103	125	mV
		Post 300 Krad(Si)	1	70	92	125	70	92	125	mV
Input Current (I_{SENSE}+) + (I_{SENSE}-) ②	$V_{SENSE\ (CM)}$ = 0V		1	-	705	-	-	705	-	uA
Operating Frequency	R_{SET} = 49.9KΩ		4	270	320	370	270	320	370	KHz
			5, 6	240	-	390	-	-	-	KHz
		Post 300 Krad(Si)	4	260	320	370	260	320	370	KHz
Programmable Frequency Range	F_{SW} ≤ 100kHz at R_{SET} = 232KΩ F_{SW} ≥ 500kHz at R_{SET} = 20KΩ		7, 8a, 8b	Pass	-	-	Pass	-	-	Pass/Fail
External Sync Frequency Range	100kHz ≤ F_{SYNC} ≤ 600kHz		7, 8a, 8b	Pass	-	-	Pass	-	-	Pass/Fail
Sync Voltage Threshold			1, 2, 3	-	1.4	2	-	1.4	2	V
Soft-Start Capacitor Control Current ②			1	-	11	-	-	11	-	uA
Error Amp Transconductance ②			1, 2, 3	-	450	-	-	450	-	uS
Error Amp DC Voltage Gain ②			1	-	62	-	-	62	-	dB
Error Amp Sink/Source Current ②			1	-	±30	-	-	±30	-	uA
Thermal Resistance ②	Junction to Case @ 125°C	EACH MOSFET	-	-	2.2	3.8	-	2.2	3.8	°C/W
		CONTROLLER	-	-	2.3	4.2	-	2.3	4.2	°C/W

NOTES:

① Unless otherwise specified VIN = 20V, BIAS = 10V, $\overline{SHDN} \geq 2V$, R_{SET} = 49.9KΩ, SENSE- = SENSE+ = 10V, SGND = PGND = SYNC = 0V.

② Guaranteed by design but not tested. Typical parameters are representative of device performance but are for reference only.

③ Industrial grade devices shall be tested to subgroup 1 unless otherwise specified.

④ Military grade devices ("H" and "K" suffix) shall be 100% tested to subgroups 1,2,3,4 and 7.

⑤ Subgroup 3,6 and 8 available upon request.

⑥ Subgroup 1,4,7 TC = +25°C
Subgroup 2,5,8a TC = +125°C
Subgroup 3,6,8b TC = -55°C

⑦ The -2V absolute maximum on the SWOUT pin is a transient condition. It is guaranteed by design, but not tested. Negative transients of up to -2V occur at SWOUT as part of normal operation. Direct application of power to the SWOUT pin may damage the device.

⑧ Continuous operation at or above absolute maximum ratings may adversely affect the device performance and/or life cycle.

⑨ Pre and post irradiation limits at 25°C, up to 300 Krad(Si) TID, are identical unless otherwise specified.

APPLICATION NOTES

PIN FUNCTIONS

VIN – The VIN pins are the input supply pins for the control circuitry inside the device. Decouple to SGND with a low ESR capacitor located close to the pin.

BIAS – The BIAS pins provide access to the internal 8V bias supply for decoupling and optional external sourcing. It is the power supply for most of the internal functions and the MOSFET gate drive. BIAS can only source current and may be tied to an external source to improve efficiency and allow for lower voltage operation. If BIAS is tied to an external source greater than 6.5V the device will operate with Vin as low as 4V. This configuration reduces power dissipation in the device by bypassing the internal regulator. The BIAS pin charges the bootstrapped capacitor through a diode connected to the BOOST pin. In shutdown mode the BIAS pin sinks 20µA until the pin voltage is discharged to zero volts.

NOTE: When driving VBIAS from an external source, the source must be greater than or equal to 9V and connect through a series diode.

PVIN – The PVIN pins are the power input supply for the regulator. High frequency current switching is present at this node. Decouple to PGND with a low ESR tantalum capacitors in parallel with ceramic capacitors located close to the pins.

PGND – The PGND pins are the high-current ground reference. Connect them directly to the negative side of the PVIN decoupling capacitors. Care should be taken to make sure that these currents are not referenced by the SGND pin to avoid injecting noise into the ground reference.

SGND – the SGND pins should be connected to the negative side of the VIN capacitor**.** Use a common ground plane to minimize impedance, but locate the high current fast switching devices together so their returns remain local and do not corrupt the SGND reference.

$\overline{\text{SHDN}}$ – The $\overline{\text{SHDN}}$ pin provides a method to disable the device. This pin has 125mV of hysterisis. Pull below 1.23V (nominal) to disable switching, pull above 1.35V to enable switching. Pull below one V_{BE} (0.7V nominal) to enter low power shutdown. A resistor divider to VIN can be used to set UVLO using the 1.35V threshold. When not in use, pull the pin up to VIN with a large value resistor. When exceeding the absolute maximum rating of 5V the pin voltage will be clamped at 6V nominal. Limit the current into the pin to less than 1mA to prevent overstress.

SS – The SS pin is used for soft start. It allows the user to program the rate of change of the output at start-up. The capacitance required for a given output slew rate can be calculated using the

$$SS = 11\mu A(T_{SS}/1.231V)$$

The pin should be left open if not in use.

SWOUT– The SWOUT pins are the switched output of the regulator. Connect these pins directly to the inductor of the output filter and optionally to the cathode of the schottky catch diode. The external schottky catch diode is optional.

COMP – The COMP pin provides a means to externally compensate the loop response of the controller. COMP is the output of the transconductance error amplifier. A capacitor to ground creates a pole in the control loop. A series RC creates a pole zero combination in the control loop. If the COMP pin is externally manipulated, use a series impedance of 1KΩ.

MODE – The MODE pin is used to inhibit or enable reverse current in the synchronous rectifier. Connect to VFB to inhibit reverse current. This allows discontinous current (DCM) at light loads. The PWM will skip pulses to maintain regulation. This improves efficiency at very light load. Connect MODE to VCC to enable reverse current. This allows for continuous current (CCM) at light loads. This configuration is less efficient at light loads but operates at a constant switching frequency.

$SENSE^-$- The $SENSE^-$ pin is the negative input to the current sense amplifier. The sensed inductor current limit is set to 100mV across the SENSE inputs.

$R_{SENSE} = 70mV/I_{OUT(MAX)}$

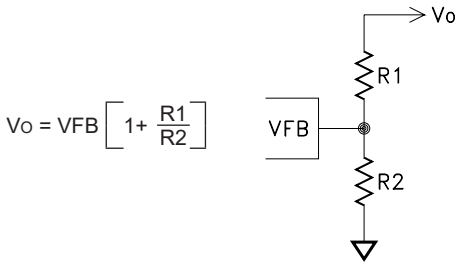
Given:
$I_{P-P} < 0.30 \times I_{OUT(MAX)}$

$SENSE^+$ - The $SENSE^+$ pin is the positive input to the current sense amplifier. The sensed inductor current limit is set to 100mV across the SENSE inputs.

$R_{SENSE} = 70mV/I_{OUT(MAX)}$

Given:
$I_{P-P} < 0.30 \times I_{OUT(MAX)}$

VFB – The VFB (Feedback) pin is used to set the output voltage. Use a resistive divider to set the voltage at the VFB pin to 1.231V when the output is at the desired level.



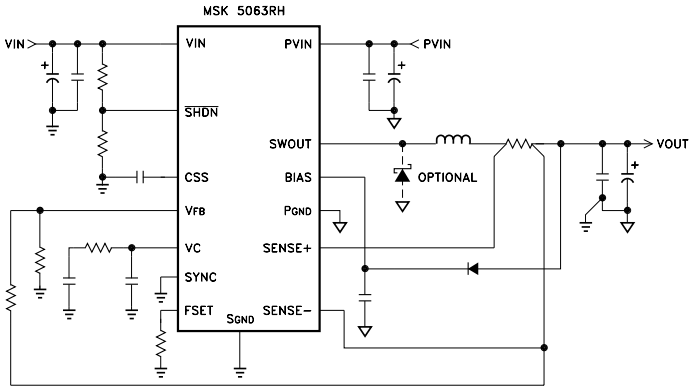
FSET – The FSET pin programs the oscillator frequency via a single resistor to ground. The R_{SET} resistor must be present even when synchronization mode is used—Use the formula or the table below to select the resistance value for a desired frequency.

$$R_{SET}(K\Omega) \approx 9.55 \times 10^4 \times f_{SW(KHZ)^{(-1.31)}}$$

RSET (KΩ)	FSW (KHz)
229	100
135	150
92.0	200
67.3	250
54.2	300
44.2	350
37.4	400
32.0	450
27.7	500

SYNC – The SYNC pin is the input for synchronization of the internal oscillator to an external clock. Program the internal oscillator to be between 10% and 25% below the external clock. The recommended signal is a square wave of at least 2V in amplitude, a pulse width greater than 1µS, and a rise time of less than 500nS. If the SYNC pin is not used in the application, tie it to SGND.

TYPICAL APPLICATION CIRCUIT



SELECTING THE INPUT CAPACITOR

The input capacitance provides a low impedance source to the input of the regulator. A low impedance is necessary for high speed, high efficiency switching and tight regulation. The input bus sources an average DC current while the input capacitance sources the AC component of the input current. Select the input capacitor based on voltage ripple requirements, RMS current rating and bulk capacitance. Assuming the capacitor ESR is lower than the bus impedance at the switching frequency and above, the ESR will dominate the voltage ripple.

$V_{P-P} \cong I_{P-P} \times ESR$

Given: $I_{P-P} = I_{OUT}$

The RMS current capability is related to power dissipation capability of the capacitor. Replace the capacitor with one that has a higher rating, or place more capacitors in parallel if more capability is needed. Sharing of ripple current between capacitors will be approximately equal if all of the capacitors are the same type, and preferably from the same lot. The RMS current seen by the input capacitors can be approximated by the following equation:

$I_{RMS} \cong I_{OUT} \times SQRT\ (3D^2 - 3D + 1)$

Given: $D \cong V_{OUT}/V_{IN}$

Parallel ceramic capacitors are required to filter the high frequency components of the switching waveform. Locate the bias supply capacitors close to the VIN and SGND pins on the MSK5063RH. Locate the power input capacitors close to the drain of the forward switch (PVIN) and the source of the synchronous rectifier (Power Ground). Use short, wide PCB lands to minimize parasitic impedances.

SELECTING THE SWITCHING FREQUENCY

The MSK5063RH can be set to operate over a frequency range of 100KHz to 500KHz, and is synchronizeable up to 600KHz. There are several factors to consider when selecting the operating frequency including: efficiency, component size, output ripple, application sensitive frequency bands, and the minimum on time of the controller. The output ripple voltage and efficiency will vary with frequency and input voltage. Higher frequencies increase switching losses, but use smaller inductors and/or bulk capacitors saving board space. Lower frequencies reduce switching losses, but increase ripple current and require larger inductors and/or bulk capacitance to achieve the same output ripple voltage.

SELECTING THE OUTPUT CAPACITOR

The output capacitor filters the ripple current from the inductor to an acceptable ripple voltage seen by the load. The primary factor in determining voltage ripple is the ESR of the output capacitor. The voltage ripple can be approximated as follows:

$$V_{P-P} = I_{P-P} \times ESR$$

The capacitive term of the output voltage ripple lags the ESR term by 90° and can be calculated as follows:

$$V_{P-P(CAP)} = I_{P-P}/ (8 \times f \times c)$$

Where:
C = output capacitance in Farads

Select a capacitor or combination of capacitors that can tolerate the worst-case ripple current with sufficient de-rating. When using multiple capacitors in parallel to achieve lower ESR or more bulk capacitance, sharing of ripple current between capacitors will be approximately equal if all of the capacitors are the same type, and preferably from the same lot. Low ESR tantalum capacitors are recommended over aluminum electrolytic capacitors. Use ceramic decoupling capacitors to minimize high frequency noise.

COMPENSATING THE LOOP

The feedback loop response can be optimized for the application by adjusting the values of the RC network from the COMP pin to ground. Analysis is recommended to determine the phase margin and gain margin at the specific input voltage and load conditions of the application. Typically, a single RC network from COMP to ground works well. An additional ceramic capacitor from COMP to ground may be needed to cancel the zero and prevent high frequency ringing or instability.

SELECTING THE INDUCTOR

The important parameters for inductor selection are: its value, volt-second product, saturation and RMS current. To determine the peak current in the inductor add ½ of the p-p ripple current to the desired IOUT(MAX). A typical starting point for peak to peak current ripple is 20% of IOUT(MAX). Use the following equation to determine the RMS current:

$$I_{RMS} = I_{DC} * SQRT (1+ (1/3) * (\Delta I/I_{DC})^2)$$

Given:
I_{DC} = The DC output current
ΔI = ½ of the peak to peak ripple current

The minimum inductance value can be calculated as follows:

$$L_{MIN} > V_{OUT} \times \frac{2DC_{MAX}-1}{DC_{MAX}} \times \frac{R_{SENSE} \times 8.33}{f_{SW}}$$

Given:
DC = Duty Cycle = V_{OUT}/V_{IN}
f_{SW} = Switching Frequency

This calculation also accommodates the max ripple/DC requirements for the slope compensation circuit.

The volt-seconds product can be calculated as follows:

$$V*S = V_I \times dt$$

Given:
V_I = the inductor voltage ($V_{IN} – V_O$)
dt = $V_O/(V_{IN} \times f_{SW})$

Allow sufficient derating to prevent saturation and/or overstress when selecting the inductor.

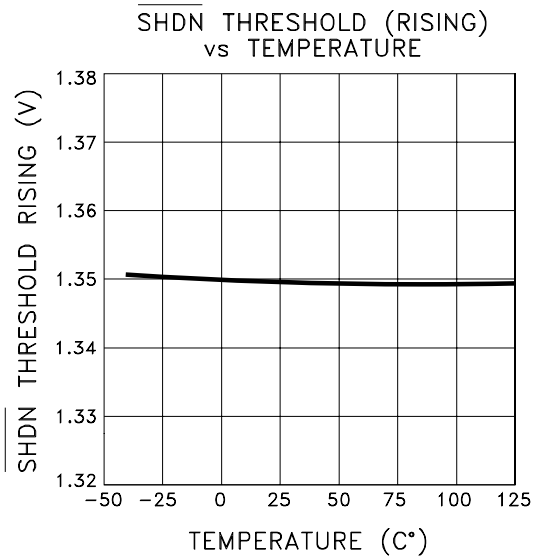
TOTAL DOSE RADIATION TEST PERFORMANCE

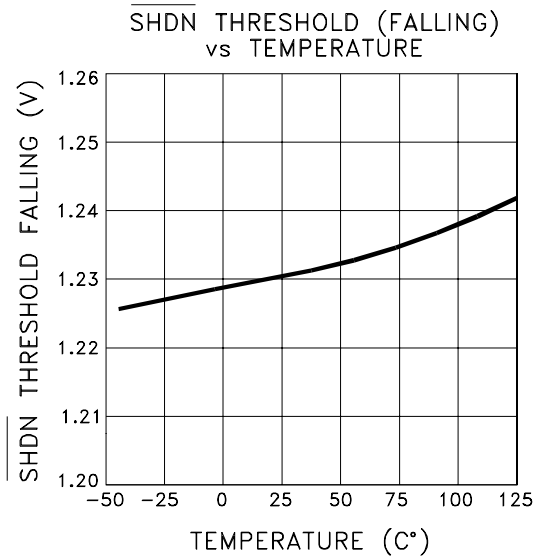
Radiation performance curves for TID testing have been generated for all testing performed by TTM Technologies. These curves show performance trends throughout the TID process, and will be located in the MSK5063RH radiation test report. The complete test report will be available in the RAD HARD PRODUCTS section of the TTM Technologies website.

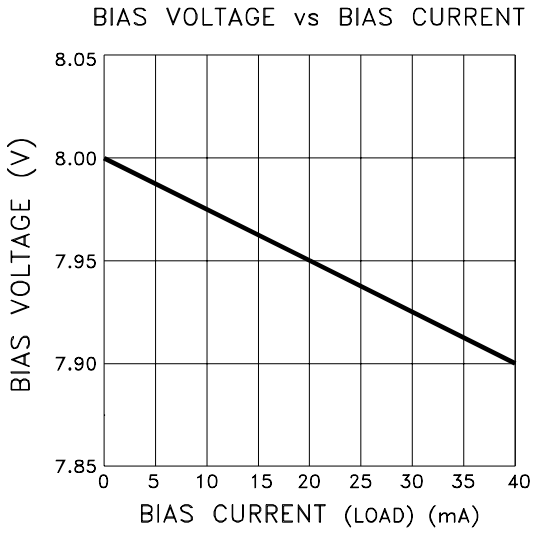
ADDITIONAL APPLICATION INFORMATION

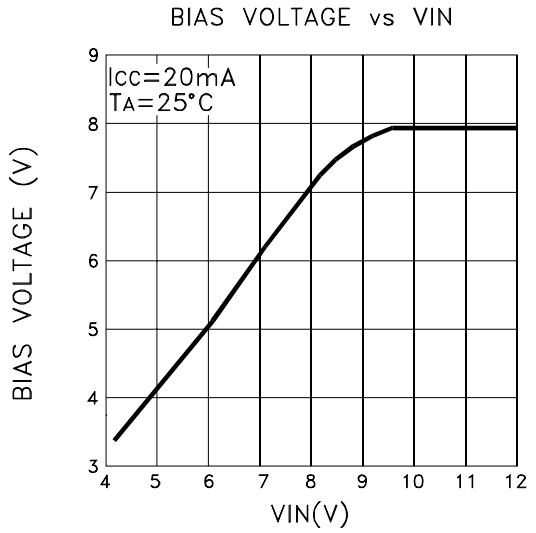
For additional applications information, please reference Linear Technology's® LT3845 data sheet.

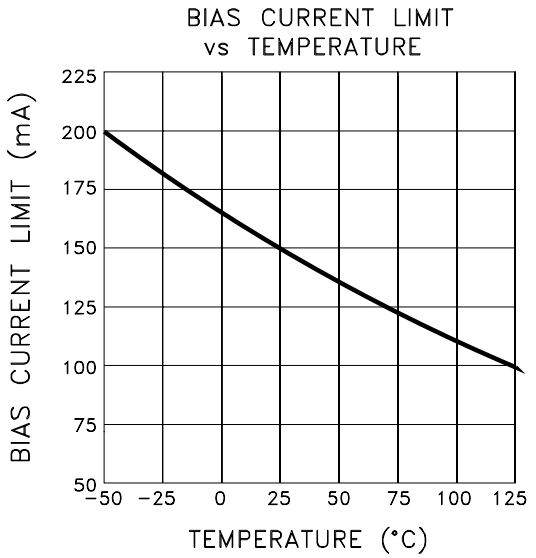
TYPICAL PERFORMANCE CURVES

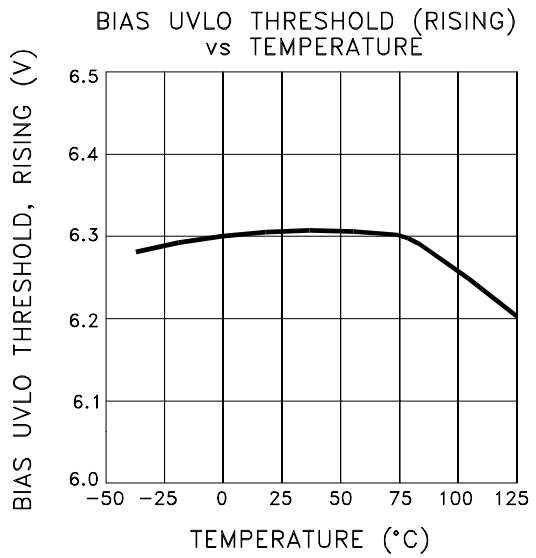




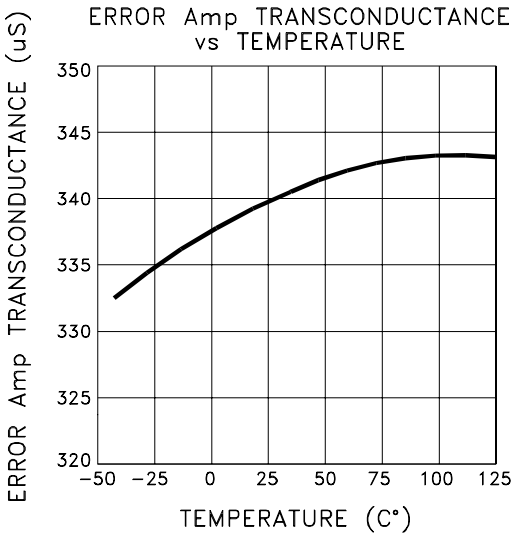


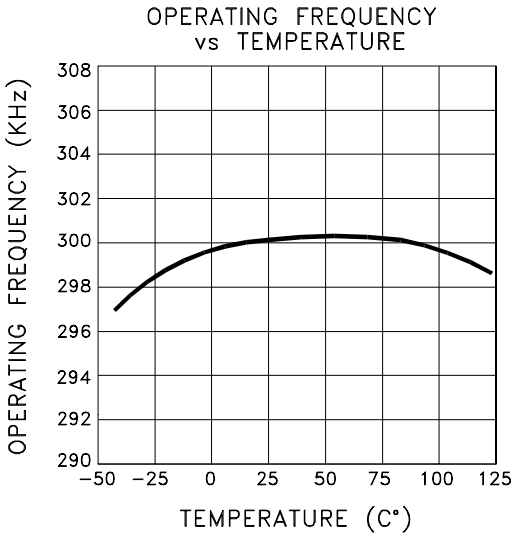


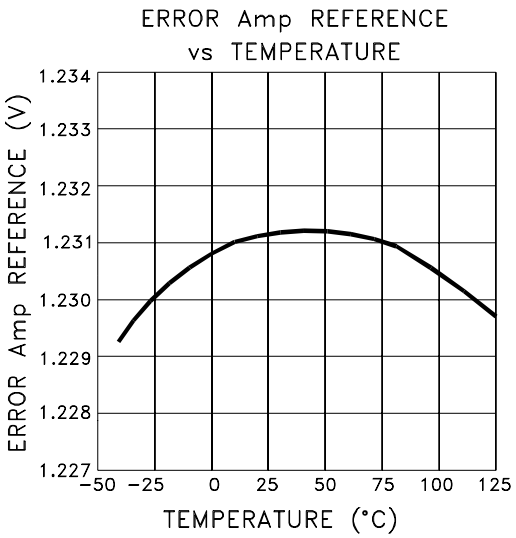


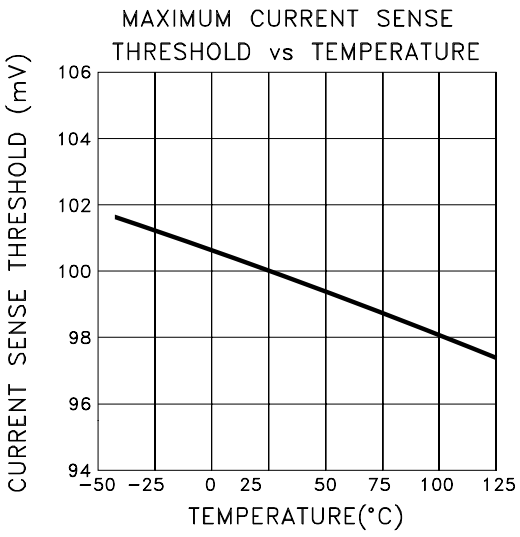


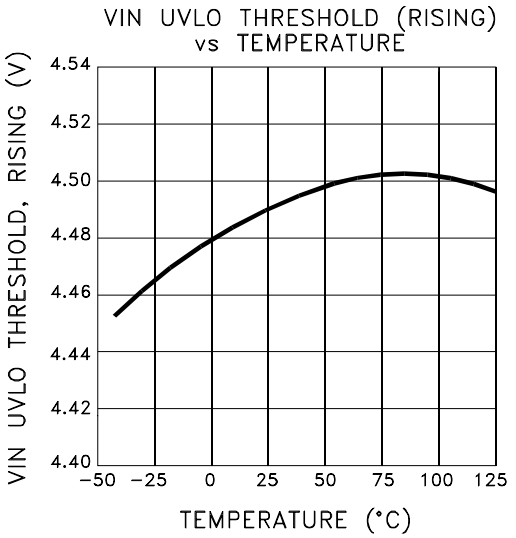
TYPICAL PERFORMANCE CURVES CONT'D

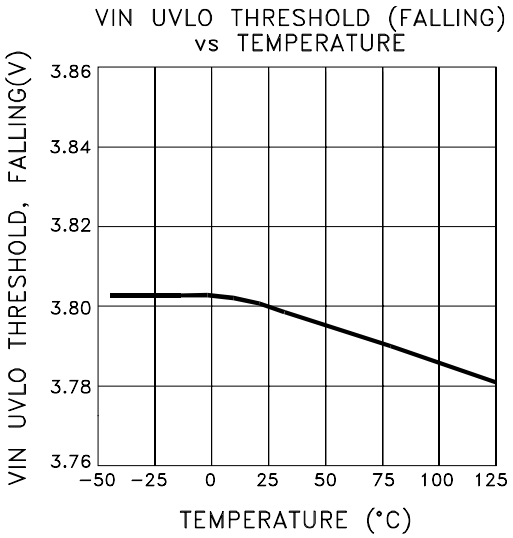




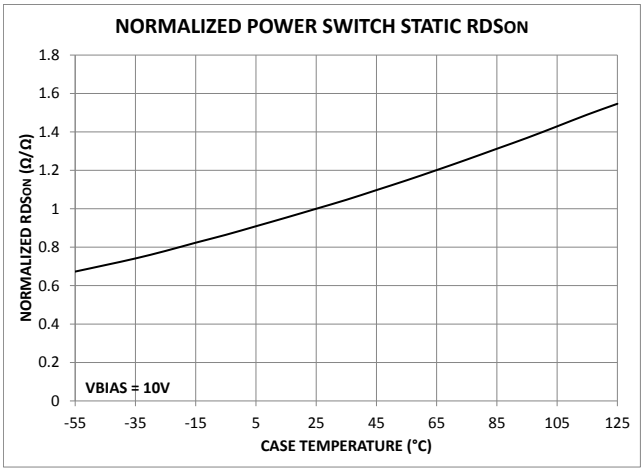


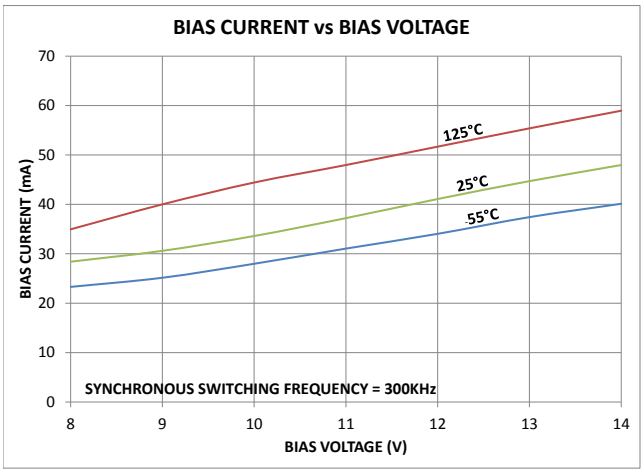


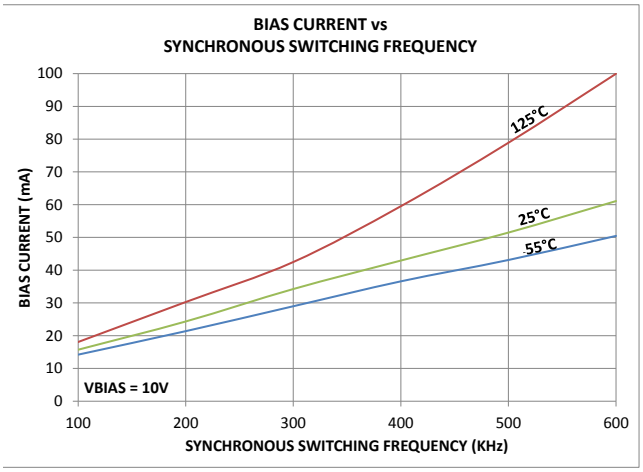


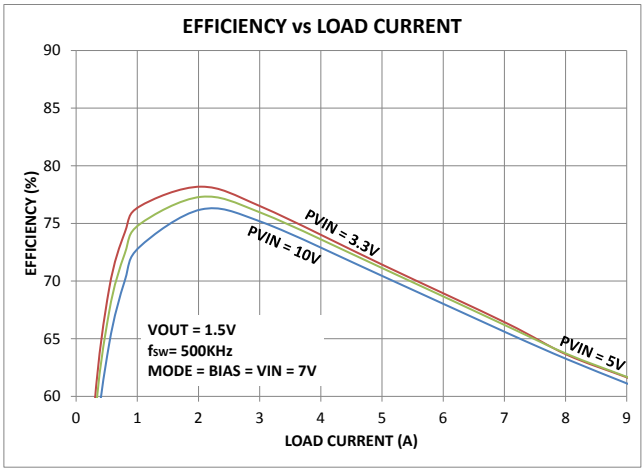


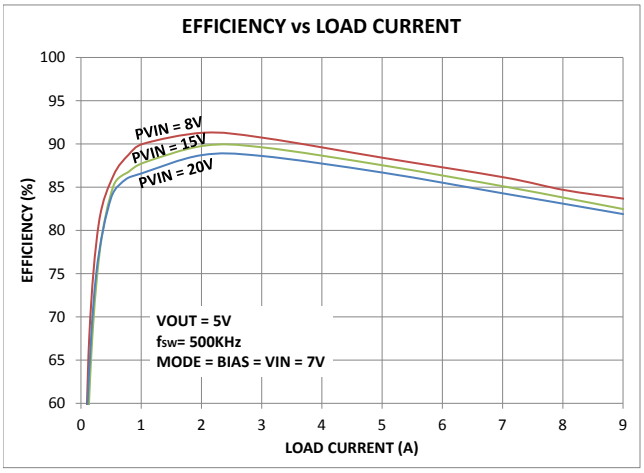
TYPICAL PERFORMANCE CURVES CONT'D

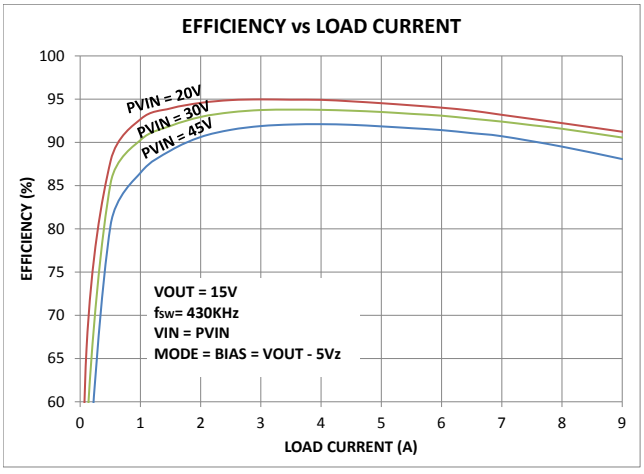




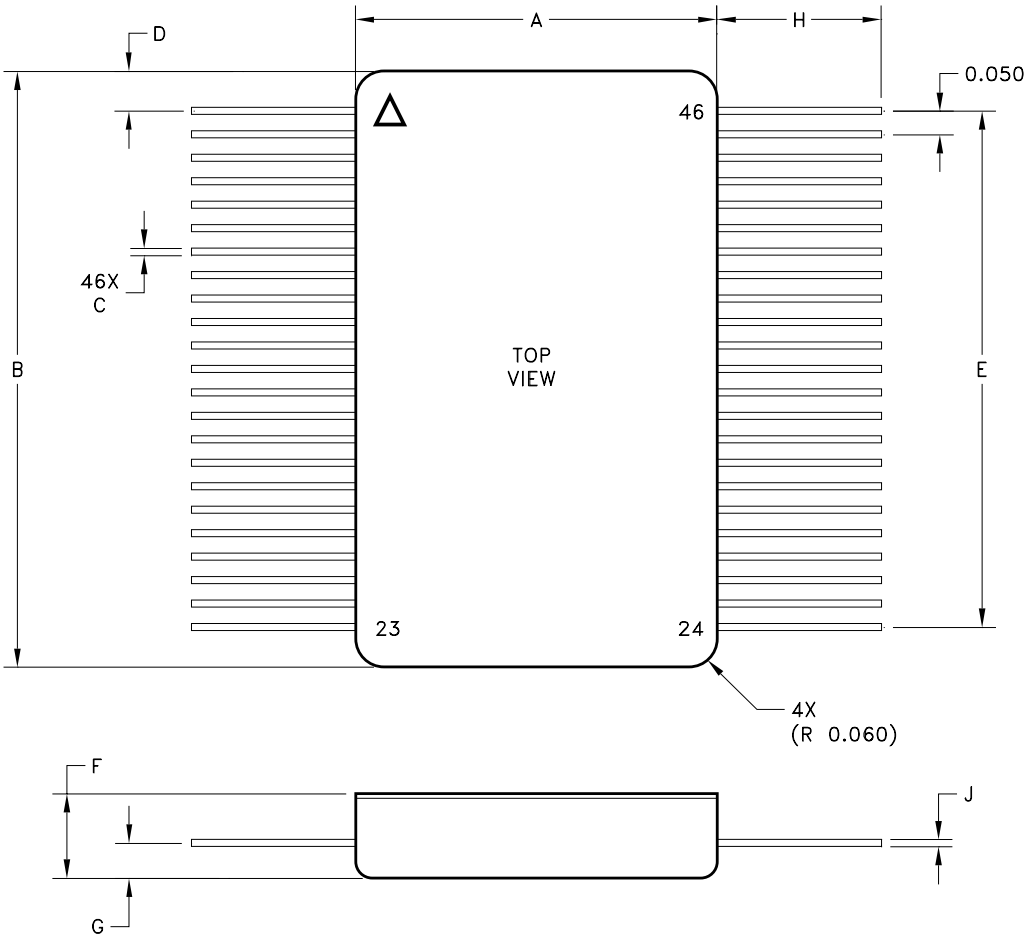








MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.760	0.780
B	1.260	1.280
C	0.012	0.018
D	0.075	0.095
E	1.095	1.105
F	———	0.180
G	0.055	0.095
H	0.350	———
J	0.008	0.012

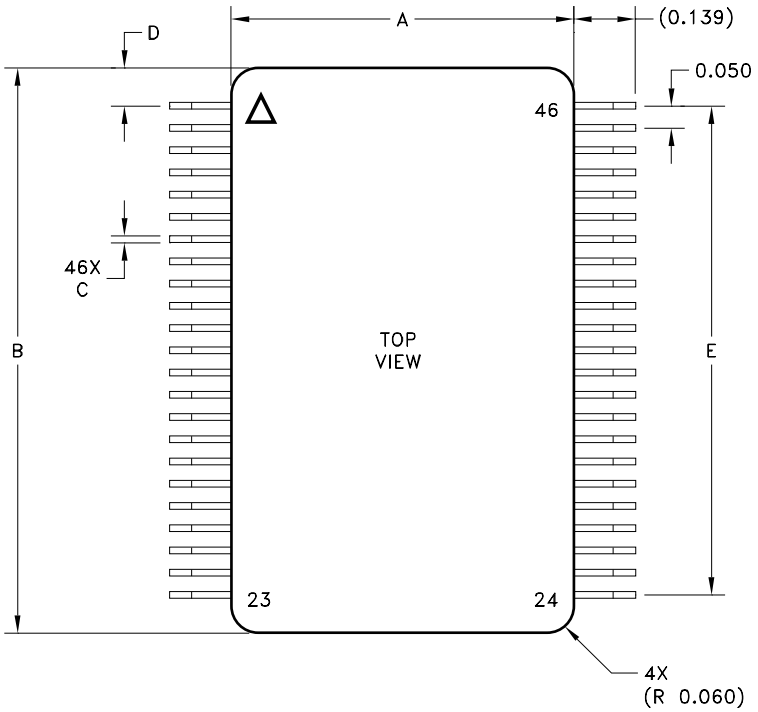
ESD TRIANGLE INDICATES PIN 1
WEIGHT = 9.4 GRAMS TYPICAL

DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5063 K RH

LEAD CONFIGURATIONS
BLANK = STRAIGHT
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
GENERAL PART NUMBER



REF	MIN	MAX
A	0.760	0.780
B	1.260	1.280
C	0.012	0.018
D	0.075	0.095
E	1.095	1.105
F	———	0.180
G	1.028	1.068
H	0.003	0.017
J	0.008	0.012
K	0.050	0.070

NOTE:

1 **'H' IS MEASURED FROM BOTTOM OF LEAD TO BOTTOM OF PACKAGE.**

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 9.3 GRAMS TYPICAL

DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5063 K RH G

LEAD CONFIGURATIONS
G = GULL WING
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H;
K = MIL-PRF-38534 CLASS K
GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
B	Released	02/14	Release data sheet, add form #, update bias supply current, add performance curves
C	Released	08/14	Update post rad specifications, add efficiency curves.
D	Released	07/15	Revise switching frequency limits update format.
E	Released	09/15	Add ESD rating, correct VFB application note.
F	Released	04/16	Update specifications, clarification of application notes.
G	Released	03/18	Update to match manufacturer's specs.
H	Released	03/22	Remove MIL-PRF-38535, update company name and website