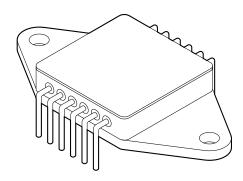
## TTM Technologies

# HIGH POWER OPERATIONAL AMPLIFIER

## 115

#### FEATURES:

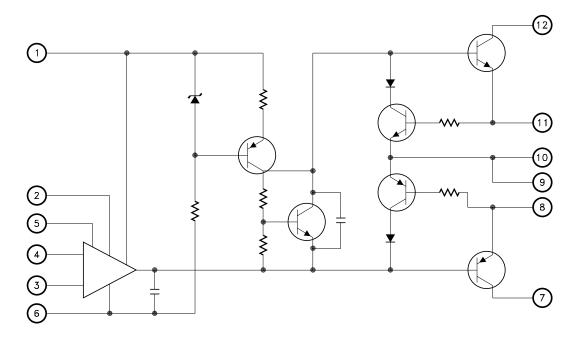
- · High Output Current 15A peak
- Ultra Low Thermal Resistance 0.5°C/W Typ.
- · Excellent Linearity Class A/B Output
- Wide Supply Range ±10V to ±50V
- · High Output Power Dissipation Capability
- · Output Short Circuit Protected
- · User Programmable Current Limit
- · Isolated Case Allows Direct Heat Sinking
- Low Quiescent Current -±22mA. Typ.
- · Contact MSK for MIL-PRF-38534 Qualification Status



#### **DESCRIPTION:**

The MSK115 is a High Power Operational Amplifier. Due to the extremely low thermal resistance from the transistor junctions to the case, the MSK115 can dissipate extreme amounts of power at a case temperature of 125°C. The amplifier

#### **EQUIVALENT SCHEMATIC**



### **TYPICAL APPLICATIONS**

- · Magnetic Deflection Circuit Driver
- Programmable Power Supplies
- · Motor, Valve and Actuator Control
- · Audio Amplifier

#### PIN-OUT INFORMATION

1 +Vcc 12 +Vc

2 Balance 11 +Current Limit

3 Inverting Input 10 Output

Non-Inverting Input 9 Output

Balance 8 -Current Limit

6 -Vcc 7 -Vc

## ABSOLUTE MAXIMUM RATINGS

8

±Vcc	Supply Voltage±50V	TST Storage Temperature Range65°C to +150°C
Iout	Output Current	TLD Lead Temperature Range
VIN	Differential Input Voltage ±37V	(10 Seconds)300°C
Tc	Case Operating Temperature Range	PD Power Dissipation See S0A Curve
	MSK115B55°C to+125°C	
	MSK11540°C to +85°C	

## **ELECTRICAL SPECIFICATIONS**

Parameter	Test Conditions (1)	Group A	MSK115B			MSK115			Units
raiametei	rest colluitions (1)	Subgroup	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
STATIC									
Supply Voltage Range ③		-	±10	-	±50	±10	-	±45	V
Quiescent Current	V <sub>IN</sub> = 0V	1	-	±22	±35	-	±22	±40	mA
Quiescent Current	Av = -10V/V	2, 3	-	±28	±45	-	-	-	mA
Thermal Resistance ③	Junction to Case @ 25°C	-	-	0.5	0.6	-	0.5	0.7	°C/W
INPUT									
1	V <sub>IN</sub> = 0V A <sub>V</sub> = 10V/V	1	-	±2	±6	-	±2	±10	mV
Input Offset Voltage	Bal. Pins = NC	2, 3	-	±3	±12	-	-	-	mV
Innuit Officet Adjust	Rpot = 10KΩ Wiper to -Vcc	7	Adjust to zero			Adjust to zero			mV
Input Offset Adjust	Av = -10V/V	8A, 8B Adjust to zero		ero	-	-	-	mV	
Innut Bing Comment	V <sub>CM</sub> = 0V	1	-	±10	±30	-	±10	±50	nA
Input Bias Current	Either Input	2, 3	-	±15	±250	-	-	-	nA
land Offer to Comment	V <sub>CM</sub> = 0V	1	-	±5	±30	-	±5	±50	nA
Input Offset Current		2, 3	-	±10	±100	-	-	-	nA
Input Impedance (3)	F = DC	-	50	250	-	35	250	-	ΜΩ
Common Mode Range (3)		-	-	±35	-	-	±35	-	V
Common Mode Rejection Ratio (3)	F = 100Hz VcM = ±5V	-	80	100	-	74	100	-	dB
OUTPUT									
0 + 17/11 0 :	$R_L = 500\Omega$ $A_V = -10V/V$	4	±35	±37	-	±33	±37	-	V
Output Voltage Swing —	$R_L = 10\Omega$ Rsc = $0\Omega$	-	±35	±36	-	±33	±36	-	V
Output Current, Peak	Av = -10V/V Vout = MAX	4	15	-	-	10	-	-	Α
Settling Time (2)(3)	0.1% 10V step	-	-	2	-	-	5	-	μS
TRANSFER CHARACTERISTICS									
Slew Rate	$V_{OUT} = \pm 10V R_L = 500\Omega A_V = -10V/V$	4	2.5	5	-	1	2.5	-	V/µS
Open Loop Voltage Gain (3)	$R_L = 500\Omega$ F = $10Hz$	4	95	105	-	85	105	-	dB
Gain Bandwidth Product (3)	$R_L = 10\Omega$ F = 1 MHz	-	-	4	-	-	3	-	MHz

#### NOTES:

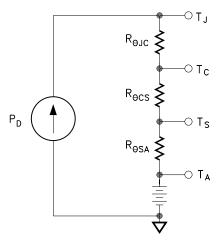
- 1 Unless otherwise specified, ±Vcc = ±40VDC.
- 2 AV = -1, measured in false summing junction circuit.
- 3 Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
- (4) Industrial grade devices shall be tested to subgroups 1, 4 and 7 unless otherwise specified.
- (5) Military grade devices ("B" suffix) shall be 100% tested to subgroups 1, 2, 3, 4, 7, 8A and 8B.
- (6) Subgroups 5 and 6 testing available upon request.
- 7 Subgroup 1, 4, 7 TA = TC = +25°C 2, 5, 8A TA = TC = +125°C 3, 6, 8B TA = TC = -55°C
- (8) Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.
- 9 Internal solder reflow temperature is 180°C, do not exceed.

#### **APPLICATION NOTES**

#### **HEAT SINKING**

To determine if a heat sink is necessary for your application and if so, what type, refer to the thermal model and governing equation below.

#### Thermal Model:



#### Governing Equation:

 $TJ = PD x (R_{\theta}JC + R_{\theta}CS + R_{\theta}SA) + TA$ 

#### Where:

T<sub>J</sub> = Junction Temperature

PD = Total Power Dissipation

Rejc = Junction to Case Thermal Resistance

Recs = Case to Heat Sink Thermal Resistance

Resa = Heat Sink to Ambient Thermal Resistance

Tc = Case Temperature

TA = Ambient Temperature

Ts = Sink Temperature

#### Example:

In our example the amplifier application requires the output to drive a 20 volt peak sine wave across a 20 ohm load for 1 amp of output current. For a worst case analysis we will treat the 1 amp peak output current as a D.C. output current. The power supplies are ±40 VDC.

1.) Find Power Dissipation

PD = [(quiescent current) x (Vs-(Vs))]+[(+Vs-Vo) x IOUT]

 $= (25mA) \times (80V) + (20V) \times (1A)$ 

= 2W+20W

= 22W

2.) For conservative design, set T<sub>J</sub> = +125°C

3.) For this example, worst case TA = +50°C

4.) RθJC = 0.55°C/W from MSK 115B Data Sheet

5.) R $\theta$ CS = 0.15°C/W for most thermal greases

6.) Rearrange governing equation to solve for Resa

Resa =  $((T_J-T_A)/P_D) - (R_{\theta}J_C) - (R_{\theta}C_S)$ =  $((125^{\circ}C - 50^{\circ}C)/22W) - (0.55^{\circ}C/W) - (0.15^{\circ}C/W)$ =  $2.71^{\circ}C/W$ 

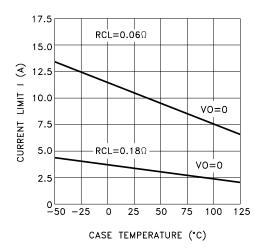
The heat sink in this example must have a thermal resistance of no more than 2.71°C/W to maintain a junction temperature of no more than +125°C.

#### **CURRENT LIMIT**

The MSK115 has an on-board current limit scheme designed to shut off the output drivers anytime output current exceeds a predetermined limit. The following formula may be used to determine the value of current limit resistance necessary to establish the desired current limit.

RcL=(OHMs)=(0.65 volts/current limit in amps) - 0.01OHM

The 0.01 ohm term takes into account any wire bond and lead resistance. Since the 0.65 volt term is obtained from the base emitter voltage drop of a bipolar transistor: the equation only holds true for operation at  $+25^{\circ}$ C case temperature. The curve below illustrates the effect of case temperature on current limit.



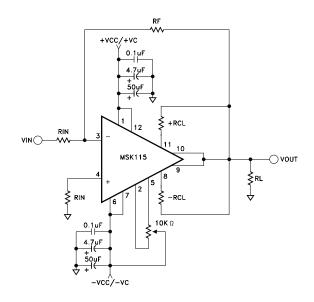
#### POWER SUPPLY BYPASSING

Both the negative and the positive power supplies must be effectively decoupled with a high and low frequency bypass circuit to avoid power supply induced oscillation. An effective decoupling scheme consists of a 0.1 microfarad ceramic capacitor in parallel with a 4.7 microfarad tantalum capacitor from each power supply pin to ground. It is also a good practice with very high power op-amps, such as the MSK115, to place a 30-50 microfarad nonelectrolytic capacitor with a low effective series resistance in parallel with the other two power supply decoupling capacitors. This capacitor will eliminate any peak output voltage clipping which may occur due to poor power supply load regulation. All power supply decoupling capacitors should be placed as close to the output stage power supply pins as possible (pins 7 and 12).

## APPLICATION NOTES CONT'D

#### **BALANCE PINS**

Pins 2 & 5 of the MSK115 are used to null unwanted input offset voltage. Connect as shown in the typical connection schematic. If the balance pins are not used, they should be left open/not connected.

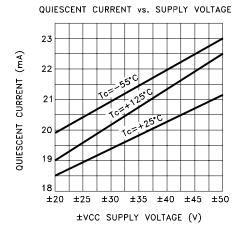


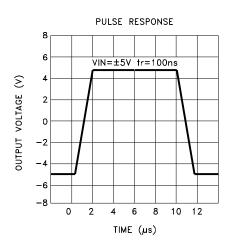
PIN DESCRIPTIONS				
NUMBER	NAME	FUNCTION		
1	1 +VCC	POSITIVE SUPPLY VOLTAGE FOR FRONT END OP-AMP		
2	BALANCE	USED TO PROVIDE OFFSET VOLTAGE NULL, SEE APPLICATION NOTES		
3	INVERTING INPUT	INVERTING INPUT FOR THE OP-AMP		
4	NON-INVERTING INPUT	NON-INVERTING INPUT FOR THE OP-AMP		
5	BALANCE	USED TO PROVIDE OFFSET VOLTAGE NULL, SEE APPLICATION NOTES		
6	① -VCC	NEGATIVE SUPPLY VOLTAGE FOR FRONT END OP-AMP		
7	① -VC	POWER SUPPLY CONNECTION TO THE COLLECTOR OF THE NEGATIVE OUTPUT TRANSISTOR. PROVIDES OUTPTU VOLTAGE/CURRENT.		
8	-CURRENT LIMIT (-CL)	USED TO PROVIDE CURRENT LIMIT PROTECTION TO THE NEGATIVE OUTPUT TRANSISTOR.		
9	OUTPUT	OP-AMP OUTPUT, CONNECT TO PIN 10 EXTERNALLY.		
10	OUTPUT	OP-AMP OUTPUT, CONNECT TO PIN 9 EXTERNALLY.		
11	+CURRENT LIMIT (+CL)	USED TO PROVIDE CURRENT LIMIT PROTECTION TO THE POSITIVE OUTPUT TRANSISTOR		
12	① +VC	POWER SUPPLY CONNECTION TO THE COLLECTOR OF THE POSITIVE OUTPUT TRANSISTOR. PROVIDES OUTPUT VOLTAGE/CURRENT.		

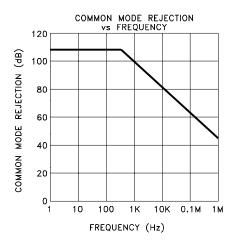
① THE OUTPUT STAGE COLLECTORS (VC) ARE NORMALLY CONNECTED TO THE CORRESPONDING VCC PINS EXTERNALLY.

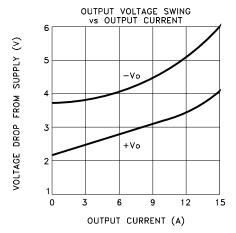
THEY ARE BROUGHT OUT ON SEPERATE PINS FOR FLEXIBILITY FR THE USER.

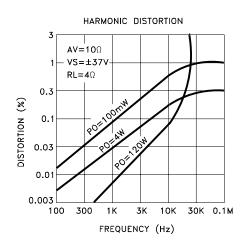
## TYPICAL PERFORMANCE CURVES

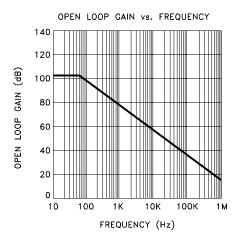


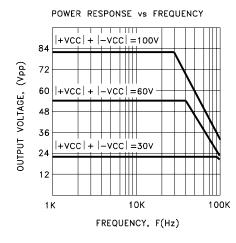


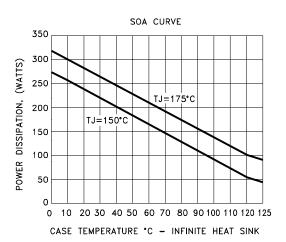






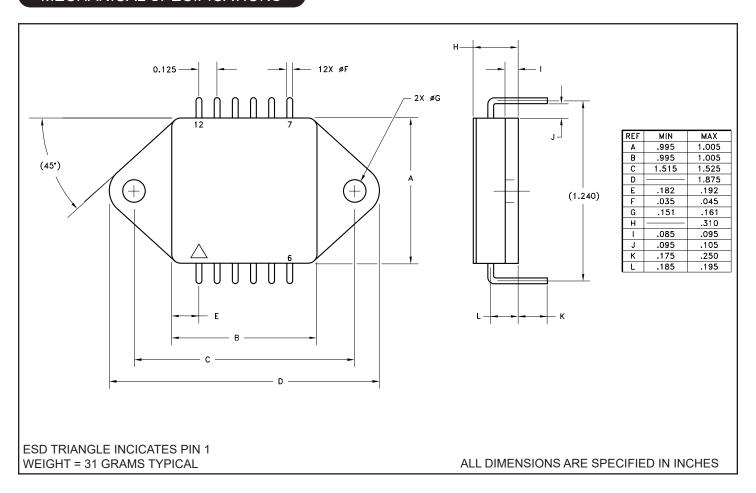






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MECHANICAL SPECIFICATIONS



## **ORDERING INFORMATION**

Part Number	Screening Level
MSK115	Industrial
MSK115B	MIL-PRF-38534 Class H

## **REVISION HISTORY**

REV	STATUS	DATE	DESCRIPTION
E	Released	04/14	Add form #, update thermal specifications, add new note for solder reflow and clarify mechanical specifications
F	Released	09/21	Remove MIL-PRF-38535

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