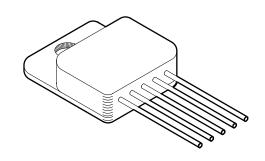
TTM Technologies

RAD HARD ULTRA LOW DROPOUT POSITIVE LINEAR REGULATOR

5822R

FEATURES:

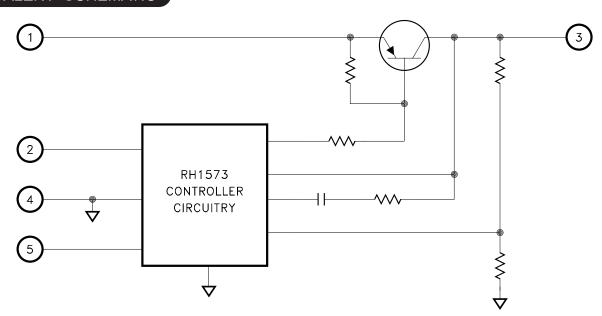
- Manufactured using.
 - OGY Space Qualified RH1573 Die
- New "Harder" Version of MSK5922RH
- Total Dose Hardened to 300 Krads(Si) (Method 1019.7 Condition A)
- Low Dropout for Reduced Power Consumption
- · Latching Overload Protection
- Available in 1.5V,1.9V,2.5V,2.8V,3.3V and 5.0V Output Voltages
- Alternate Output Voltages Available
- · Output Current Limit
- Available in 3 Lead Form Options: Straight, Up and Down
- · Seperate Bias/Vin Pins for Improved Efficiency
- Available to DLA SMD 5962F09236
- ELDRS Tested to 100 Krads(Si) (Method 1019.7 Condition D)
- Neutron Tested to 1.0x10¹² n/cm² (Method 1017.2)



DESCRIPTION:

The MSK5822RH is a rad hard fixed linear regulator capable of delivering 5.0 amps of output current. Typical dropout is only 0.35 volts with a 2.5 amp load. Separated power and bias simplifies supply tracking. This device also has latching overload protection. The MSK5822RH is radiation hardened and specifically designed for space/satellite applications. The device is packaged in a hermetically sealed space efficient 5 pin SIP that is electrically isolated from the internal circuitry allowing for direct heat sinking.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Satellite System Power Supplies
- Switching Power Supply Post Regulators
- · Constant Voltage/Current Regulators
- Microprocessor Power Supplies

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PIN-OUT INFORMATION

- VIN
- 2 **VBIAS**
- **VOUT**
- **GND**
- LATCH

CASE = ISOLATED

ABSOLUTE MAXIMUM RATINGS

(8)

VBIAS	Bias Supply Voltage+10V	Tst	Storage Temperature Range 365°C to +150°C
VIN	Supply Voltage+10V	TLD	Lead Temperature Range
IOUT	Output Current 7		(10 Seconds) 300°C
Tc	Case Operating Temperature Range	PD	Power Dissipation See SOA Curve
	MSK5822K/H RH55°C to +125°C	TJ	Junction Temperature 150°C
	MSK5822RH -40°C to +85°C		

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions ① ⑨ ①		Group A	MSK5822K/H RH		MSK5822RH			Units	
Parameter			Subgroup	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Input Voltage Range 2	10mA ≤ lout	≤ 1.0A	1, 2, 3	2.0	-	6.5	2.0	-	6.5	V
Input Bias Voltage 2	VBIAS ≥	VIN	1, 2, 3	2.9	5.0	6.5	2.9	5.0	6.5	V
Quiescent Current	IIN + IBIAS, VBIAS : Not Includin		1, 2, 3	-	14	20	-	14	20	mA
Bias Current	VBIAS = 6	6.5V	1, 2, 3	-	2	4	-	2	4	mA
	VIN = VOUT + 1V		1	-	±0.1	±1.0	-	±0.1	±1.5	%
Output Voltage Telerance	Iout = 1A		2, 3	-	-	±2.5	-	-	-	%
Output Voltage Tolerance		Post 100KRAD(Si)	1	-0.5	+0.25	+1.5	-0.5	+0.25	+1.5	%
		Post 300KRAD(Si)	1	-0.5	+1.0	+2.75	-0.5	+1.0	+2.75	%
Line Begulation	IOUT = 50mA VOUT +0.4 ≤ VIN ≤ 6.5V		1	-	±0.1	±0.50	-	0.1	±0.60	%
Line Regulation (9)			2, 3	-	-	±2.5	-	-	-	%
Load Regulation (9)	50mA ≤ Iouт ≤ 3.0A		1	-	0.66	1.0	-	0.66	1.2	%
Load Regulation (9)	VIN = VOU	T +1V	2, 3	-	-	±2.5	-	-	1	%
	Dolto VOLIT - 10/	lour = 2.5A	1	-	0.35	0.45	-	0.35	0.50	V
Dropout Voltage (10)	Delta VOUT = 1% IouT = 2.5A	1001 - 2.5A	2, 3	-	0.40	0.50	-	-	-	V
Dropout voltage (10)		Post 100KRAD(Si)	1	-	0.40	0.50	-	0.40	0.50	V
		Post 300KRAD(Si)	1	-	0.42	0.53	-	0.42	0.53	V
Output Current Limit (7) (9)	VIN = VOUT +1V Overcurrent Latch Up		1	3.0	-	5	3.0	-	5	Α
Output Current Limit (7) (9)			2, 3	3.0	-	5	-	-	-	Α
Pinnle Rejection (2)	f = 120Hz lout = 50mA		4	65	-	-	65	-	-	dB
Ripple Rejection (2)			5, 6	65	-	-	-	-	-	dB
Thermal Resistance 2	Junction to Case @ 125°C Output Device		-	-	2.2	3.0	-	2.2	3.5	°C/W

PART NUMBER	OUTPUT VOLTAGE
MSK5822-1.5	+1.5V
MSK5822-1.9	+1.9V
MSK5822-2.5	+2.5V
MSK5822-2.8	+2.8V
MSK5822-3.3	+3.3V
MSK5822-5.0	+5.0V

NOTES:

- (1) Unless otherwise specified, VIN = VOUT +1V, VBIAS = 5V and IOUT = 10mA. See Figure 2 for typical test circuit.
- (2) Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
- (3) Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise requested.
- (4) Military grade devices ("H" and "K" suffix) shall be 100% tested to subgroups 1, 2, 3 and 4.
- (5) Subgroup 5 and 6 testing available upon request.
- 6 Subgroup 1, 4 TC = +25°C Subgroup 2, 5 TC = +125°C

Subgroup 3, 6 TA = -55° C

- (7) Output current limit is dependent upon the values of VIN and VOUT. See Figure 1 and typical performance curves.
- (8) Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.
- (9) VIN shall be as specified or VIN min., whichever is greater.
- (10) Saturation voltage varies with load. See typical performance curves.
- (1) Pre and post irradiation limits, at +25°C, up to 300Krad TID, are identical unless otherwise specified.
- (12) Reference DLA SMD 5962F09236 for electrical specifications for devices purchased as such.
- (13) Internal solder reflow temperature is 180°C, do not exceed.

APPLICATION NOTES

PIN FUNCTIONS

VIN - This pin provides the input power connection to the MSK5822RH. This is the supply that will be regulated to the output. Input voltage range is VOUT + VDROPOUT to 6.5V.

VBIAS - This pin provides power to all internal circuitry including bias, start-up, thermal limit and overcurrent latch. VBIAS voltage range is 2.9V to 6.5V. VBIAS should be kept greater than or equal to VIN.

LATCH - The MSK5822RH LATCH pin is used for both current limit and thermal limit. A capacitor between the LATCH pin and ground sets a time out delay in the event of an over current or short circuit condition. The capacitor is charged to approximately 1.6V from a 7.2µA (nominal) current source. Exceeding the thermal limit charges the latch capacitor from a larger current source for a near instant shutdown. Once the latch capacitor is charged the device latches off until the latch is reset. Momentarily pull the LATCH pin low, or cycle the power to reset the latch. Cycling the bias power disables the device during the reset operation. Pulling the LATCH pin low immediately enables the device for as long as the LATCH pin is held low plus the time delay to re-charge the latch capacitor whether or not the fault has been corrected. Disable the latch feature by tying the LATCH pin low. With the LATCH pin held low the thermal limit feature is disabled and the current limit feature will force the output voltage to droop but remain active if excessive current is drawn.

GND - Internally connected to ground, this pin should be connected externally by the user to the circuit ground.

VOUT - This is the output pin for the device.

INPUT POWER SUPPLY BYPASSING

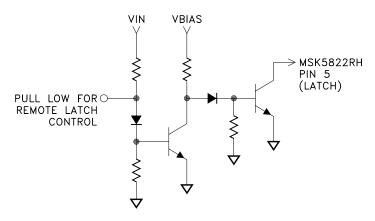
To maximize transient response and minimize power supply transients it is recommended that two $47\mu F$ tantalum capacitors are connected between VIN and ground. A $0.1\mu F$ ceramic capacitor should also be used for high frequency bypassing. See typical application circuit.

OUTPUT CAPACITOR SELECTION

Output capacitors are required to maintain regulation and stability. Between 440 and $100\mu F$ surface mount, low ESR, tantalum capacitor from the output to ground should suffice under most conditions. See typical application circuit for recommended capacitance. Ceramic output capacitors (0.1 μF typical) should be placed directly across the load power connections as close to the load as possible. If the user finds that tighter voltage regulation is needed during output transients, more capacitance may be added. If more capacitance is added to the output, the bandwidth may suffer.

START UP OPTIONS

The MSK5822RH starts up and begins regulating immediately when VBIAS and VIN are applied simultaneously. Applying VBIAS before VIN starts the MSK5822RH up in a disabled or latched state. When starting in a latched state the device output can be enabled by pulling the latch pin low to drain the latch capacitor. Hold the latch pin low and release after VIN comes up to ensure automatic startup when applying VBIAS before VIN. The basic circuit below can be adapted to a variety of applications for automatic start up when VBIAS rises before VIN.



START UP CURRENT

The MSK5822RH sinks increased current during startup to bring up the output voltage. Reference the "Saturated Drive Current vs. Input Voltage" graph in the typical performance curves of this data sheet and the "Understanding Startup Surge Current With RH1573 Based Rad Hard LDO Regulators" application note in the application notes section of the TTM Technologies Web site for more information.

OVERCURRENT LATCH-OFF/LATCH PIN CAPACITOR SELECTION

As previously mentioned, the LATCH pin provides over current/output short circuit protection with a timed latch-off circuit. Reference the LATCH pin description note. The latch off time out is determined with an external capacitor connected from the LATCH pin to ground. The time-out period is equal to the time it takes to charge this external capacitor from 0V to 1.6V. The latch charging current is provided by an internal current source. This current is a function of bias voltage and temperature (see latch charging current curve). For instance, at 25°C , the latch charging current is $7.2\mu\text{A}$ at VBIAS=3V and $8\mu\text{A}$ at VBIAS=6.5V.

In the latch-off mode, some additional current will be drawn from the bias supply. This additional latching current is also a function of bias voltage and temperature (see typical performance curves).

The MSK5822RH current limit function is directly affected by the input and output voltages. Custom current limit is available; contact the factory for more information.

THERMAL LIMITING

The MSK5822RH control circuitry has a thermal shutdown temperature of approximately 150°C. This thermal shutdown can be used as a protection feature, but for continuous operation, the junction temperature of the pass transistor must be maintained below 150°C. Proper heat sink selection is essential to maintain these conditions. Exceeding the thermal limit activates the latch feature of the MSK5822RH. Momentarily pull the latch pin low or cycle the power to reset the latch.

APPLICATION NOTES CONT'D

HEAT SINK SELECTION

To select a heat sink for the MSK5822RH, the following formula for convective heat flow may be used.

Governing Equation:

$$T_J = P_D X (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$

Where

TJ = Junction Temperature PD = Total Power Dissipation

 $R_{\theta JC}$ = Junction to Case Thermal Resistance $R_{\theta SA}$ = Case to Heat Sink Thermal Resistance Heat Sink to Ambient Thermal Resistance

TA = Ambient Temperature

Power Dissipation = (VIN-VOUT) x IOUT

Next, the user must select a maximum junction temperature. The absolute maximum allowable junction temperature is 150°C. The equation may now be rearranged to solve for the required heat sink to ambient thermal resistance ($R_{\rm PSA}$).

Example:

An MSK5822-2.5RH is connected for VIN = +3.3V and VOUT = +2.5V. IouT is a continuous 3A DC level. The ambient temperature is $+25^{\circ}$ C. The maximum desired junction temperature is $+125^{\circ}$ C.

 $R_{\theta JC} = 3.0^{\circ}\text{C/W}$ and $R_{\theta CS} = 0.15^{\circ}\text{C/W}$ for most thermal greases Power Dissipation = $(3.3\text{V}-2.5\text{V}) \times (3\text{A})$ = 2.4 Watts

Solve for Resa:

Resa =
$$\left[\frac{125^{\circ}\text{C} - 25^{\circ}\text{C}}{2.4\text{W}}\right]$$
 -3.0°C/W - 0.15°C/W
= 38.5°C/W

In this example, a heat sink with a thermal resistance of no more than 38°C/W must be used to maintain a junction temperature of no more than 125°C.

TYPICAL APPLICATIONS CIRCUIT

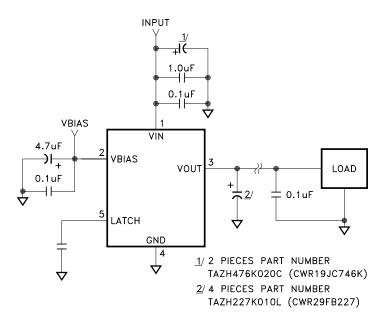


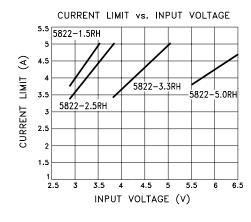
FIGURE 2

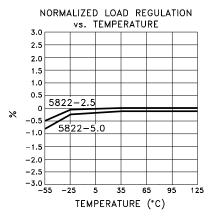
TOTAL DOSE RADIATION TEST PERFORMANCE

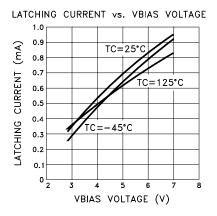
Radiation performance curves for TID testing have been generated for all radiation testing performed by TTM Technologies. These curves show performance trends throughout the TID test process and are located in the MSK5822RH radiation test report. The complete radiation test report is available in the RAD HARD PRODUCTS section on the TTM Technologies website.

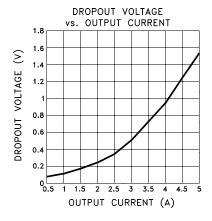
Reference the MSK5826RH RAD REPORT for ELDRS and Neutron results.

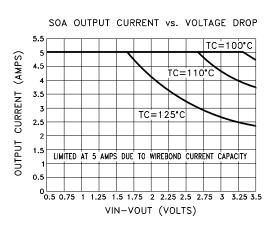
TYPICAL PERFORMANCE CURVES

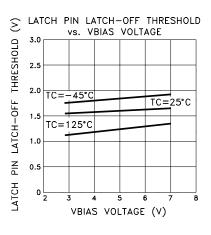


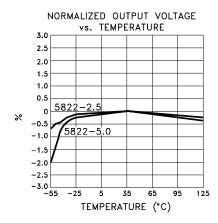


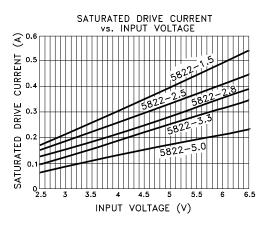


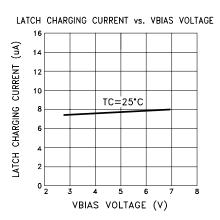








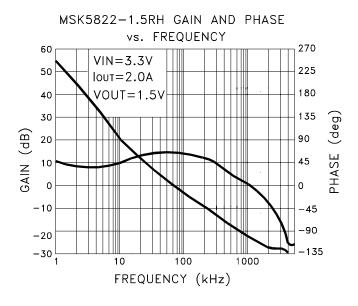


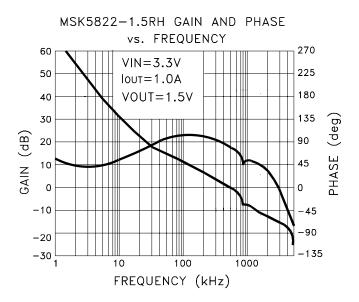


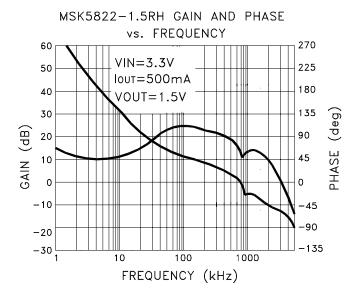
TYPICAL PERFORMANCE CURVES CONT'D

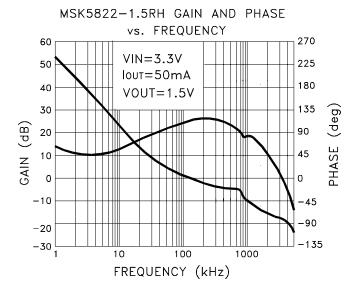
GAIN AND PHASE RESPONSE

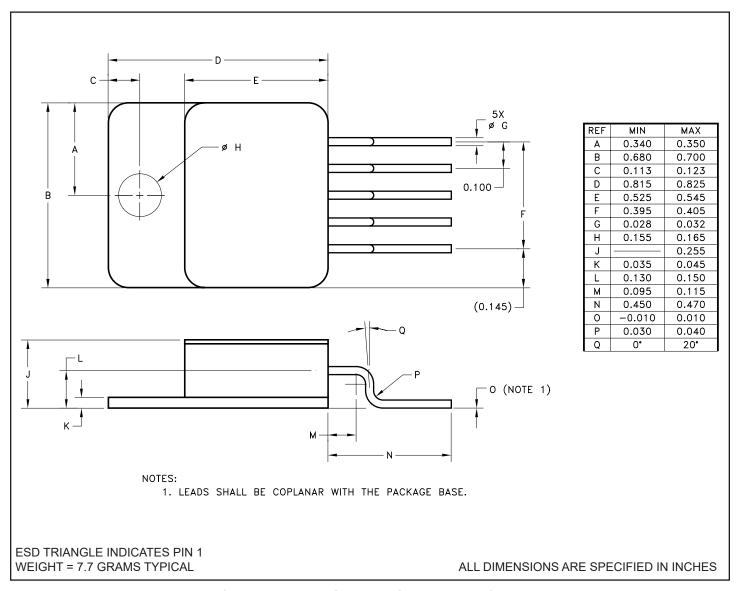
The gain and phase response curves are for the typical application circuit at 25°C and are representative of typical device performance, but are for reference only. The performance should be analyzed for each application to insure individual program requirements are met. External factors such as temperature, input and output voltages, capacitors, etc. all can be major contributors. Please consult factory for additional details.



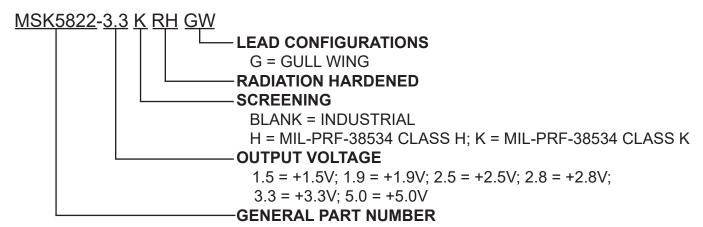






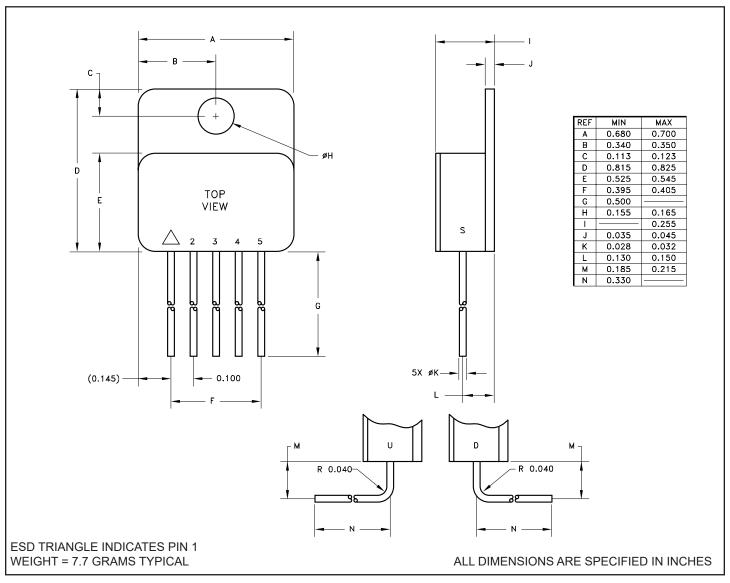


ORDERING INFORMATION

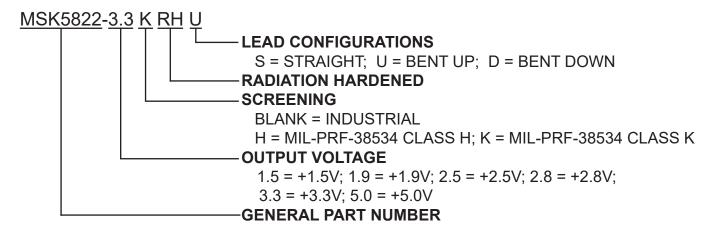


The above example is a +3.3V, Class K regulator with leads bent up. NOTE: See DLA SMD 5962F09236 for DLA part number options.

MECHANICAL SPECIFICATIONS CONT'D



ORDERING INFORMATION



The above example is a +3.3V, Class K regulator with leads bent up. NOTE: See DLA SMD 5962F09236 for DLA part number options.

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION	
I	Released	06/14	Add new note for solder reflow and clarify mechanical outline	
J	Released	03/15	Add gull wing	
K	Released	08/15	Clarify note on page 2	
L	Released	03/22	Remove MIL-PRF-38535, update company name and website	

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