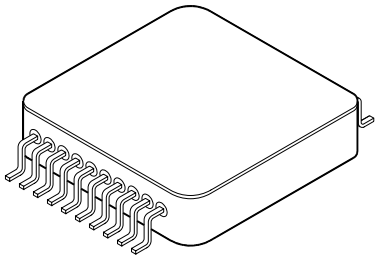
MIL-PRF-38534 CERTIFIED FACILITY

# RAD HARD ULTRA LOW VOLTAGE ADJUSTABLE POSITIVE LINEAR REGULATOR

# 5950RH

## *FEATURES:*

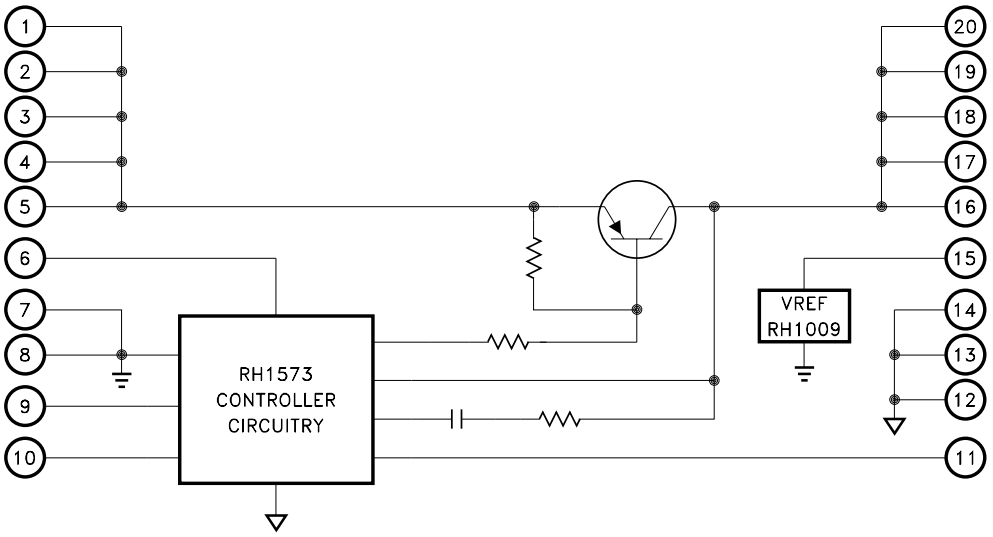
- Manufactured using LINEAR TECHNOLOGY Space Qualified RH1009 and RH1573 Die
- Total Dose Hardened to 100 Krads(Si) (Method 1019.7 Condition A)
- Total Dose Test Reports to 450 Krads(Si) available on website.
- Output Adjustable Down to Near Zero
- External Shutdown/Reset Function
- Latching Overload Protection
- Adjustable Output Using External Resistors
- Output Current Limit
- Surface Mount Package Available with Lead Forming
- Low Input Voltage for Maximum Efficiency
- Up to 5A Output Current



## *DESCRIPTION:*

The MSK5950RH is a radiation hardened adjustable linear regulator capable of delivering 5.0 amps of output current. The typical dropout is only 0.11 volts at 1 amp. An external shutdown/reset function is ideal for power supply sequencing. This device also has latching overload protection that requires no external current sense resistor. The MSK5950RH is radiation hardened and specifically designed for many space/satellite applications. The device is packaged in a hermetically sealed 20 pin flatpack that can be lead formed for surface mount applications.

## EQUIVALENT SCHEMATIC




## TYPICAL APPLICATIONS

- Satellite System Power Supplies
- Switching Power Supply Post Regulators
- Constant Voltage/Current Regulators
- Microprocessor Power Supplies

## PIN-OUT INFORMATION

| | | | |
|---|---|---|---|
| 1 | -VINA | 11 | FB |
| 2 | VINB | 12 | GND2 |
| 3 | VINC | 13 | GND2 |
| 4 | VIND | 14 | GND2 |
| 5 | VINE | 15 | VREF |
| 6 | VBIAS | 16 | VOUTA |
| 7 | GND1 | 17 | VOUTB |
| 8 | GND1 | 18 | VOUTC |
| 9 | Latch | 19 | VOUTD |
| 10 | Shutdown | 20 | VOUTE |

CASE = ISOLATED

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## ABSOLUTE MAXIMUM RATINGS ⑧

$+V_{BIAS}$ Bias Supply Voltage.....10V
$+V_{IN}$ Supply Voltage.....10V
$V_{SD}$ Shutdown Voltage.....10V
$I_{VREF}$ Reference Sink Current.....20mA
$I_{OUT}$ Output Current .....⑦.....5A
$T_C$ Case Operating Temperature Range
MSK5950K/H RH.....-55°C to +125°C
MSK5950RH.....-40°C to +85°C

$T_{ST}$ Storage Temperature Range.....-65°C to +150°C
$T_{LD}$ Lead Temperature Range
(10 Seconds).....300°C
$P_D$ Power Dissipaton.....See SOA Curve
$T_J$ Junction Temperature.....150°C
ESD Rating.....Class 1C

## ELECTRICAL SPECIFICATIONS

| Parameter | Test Conditions ① ⑨ | | Group A Subgroup | MSK5950K/H SERIES Min. | Typ. | Max. | MSK5950 SERIES Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Input Voltage Range ② | 10mA ≤ $I_{OUT}$ ≤ 1.0A | | 1, 2, 3 | 2.0 | - | 7.5 | 2.0 | - | 7.5 | V |
| Bias Supply Voltage ② | VBIAS ≥ VIN | | 1, 2, 3 | 2.9 | - | 7.5 | 2.9 | - | 7.5 | V |
| Feedback Voltage | $I_{OUT}$ = 1.0A R1 = 187Ω | | 1 | 1.225 | 1.265 | 1.305 | 1.202 | 1.265 | 1.328 | V |
| | | | 2, 3 | 1.225 | - | 1.305 | - | - | - | V |
| | | Post Radiation | 1 | 1.225 | 1.272 | 1.305 | 1.202 | 1.272 | 1.328 | V |
| VREF | $I_{REF}$ = 1mA | | 1 | 2.495 | 2.500 | 2.505 | 2.485 | 2.500 | 2.515 | V |
| | | | 2, 3 | 2.485 | - | 2.515 | - | | | V |
| | | Post Radiation | 1 | 2.493 | 2.501 | 2.508 | 2.493 | 2.501 | 2.508 | V |
| VREF Load Reg | 0.4mA ≤ $I_{REF}$ ≤ 10mA | | 1 | - | - | ±6 | - | - | ±6 | mV |
| | | | 2, 3 | - | - | ±10 | - | - | ±10 | mV |
| | | Post Radiation | 1 | - | - | ±12 | - | - | ±12 | mV |
| Feedback Pin Current ② | VFB = 1.265V 10mA ≤ $I_{OUT}$ ≤ 1.0A | | 1, 2, 3 | 0 | - | 5.0 | 0 | - | 5.0 | µA |
| Quiescent Current | $I_{IN}$ + $I_{BIAS}$, VBIAS = VIN = 5.0V Not including $I_{OUT}$ | | 1, 2, 3 | - | 8 | 15 | - | 8 | 15 | mA |
| Bias Current | VBIAS = 5.0V | | 1, 2, 3 | - | 2 | 4 | - | 2 | 4 | mA |
| Line Regulation | $I_{OUT}$ = 10mA 2.9V ≤ VIN ≤ 7.5V R1 = 187Ω | | 1 | - | ±0.01 | ±0.50 | - | ±0.01 | ±0.60 | %VOUT |
| | | | 2, 3 | - | - | ±0.50 | - | - | - | %VOUT |
| Load Regulation | 10mA ≤ $I_{OUT}$ ≤ 1.0A R1 = 976Ω | | 1 | - | ±0.06 | ±0.80 | - | ±0.06 | ±1.0 | %VOUT |
| | | | 2, 3 | - | - | ±0.80 | - | - | - | %VOUT |
| Dropout Voltage | Delta FB = 1% $I_{OUT}$ = 1.0A | | 1 | - | 0.11 | 0.40 | - | 0.11 | 0.45 | V |
| | | | 2, 3 | - | 0.14 | 0.40 | - | - | - | V |
| Minimum Output Current ② | 2.9V ≤ VIN ≤ 7.5V R1 = 187Ω | | 1 | - | 8 | 10 | - | 8 | 10 | mA |
| | | | 2, 3 | - | 9 | 10 | - | - | - | mA |
| Output Voltage Range ② | VIN = 7.5V | | - | 0 | - | 7.0 | 0 | - | 7.0 | V |
| Output Current Limit ⑦ | VIN = 2.5V VOUT = 1.5V | | 1 | 3.2 | 3.6 | 4.0 | 3.2 | - | 4.0 | A |
| | | | 2, 3 | 3.0 | - | - | - | - | - | A |
| Shutdown Threshold | VOUT ≤ 0.2V (OFF) VOUT = Nominal (ON) | | 1 | 1.0 | 1.3 | 1.6 | 1.0 | 1.3 | 1.6 | V |
| | | | 2, 3 | 1.0 | 1.3 | 1.6 | - | - | - | V |
| Shutdown Hysteresis | Difference between voltage threshold of VSDI (ON) and VSDI (OFF) | | 1 | - | 0.02 | 0.2 | - | 0.02 | 0.2 | V |
| | | | 2, 3 | - | 0.03 | 0.2 | - | - | - | V |
| Ripple Rejection ② | f = 1KHz to 10KHz 10mA ≤ $I_{OUT}$≤ 1.0A 1.0V = VIN-VOUT | | 4 | 20 | - | - | 20 | - | - | dB |
| | | | 5, 6 | 20 | - | - | - | - | - | dB |
| Phase Margin ② | $I_{OUT}$ = 450mA | | 4, 5, 6 | 30 | 80 | - | 30 | 80 | - | degrees |
| Gain Margin ② | $I_{OUT}$ = 450mA | | 4, 5, 6 | 10 | 30 | - | 10 | 30 | - | dB |
| Equivalent Noise Voltage ② | Referred to Feedback Pin | | 4, 5, 6 | - | - | 50 | - | - | 50 | µVRMS |
| Thermal Resistance ② | Junction to Case @ 125°C Output Device | | - | - | 7.3 | 8.4 | - | 7.3 | 9.0 | °C/W |

*NOTES:*

① Unless otherwise specified, $V_{BIAS}$ = VIN = 5.0V, R1 = 1.62K, $R_{REF}$ = 249W (see figure 2), $V_{SHUTDOWN}$ = 0V and $I_{OUT}$ = 10mA.

② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only. Not applicable to post irradiation performance.

③ Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise requested.

④ Military grade devices ("H" suffix) shall be 100% tested to subgroups 1,2,3 and 4.

⑤ Subgroup 5 and 6 testing available upon request.4

⑥ Subgroup 1, 4 $T_A$ = +25°C
2, 5 $T_A$ = +125°C
3, 6 $T_A$ = -55°C

⑦ Output current limit is tested with a low duty cycle pulse to minimize junction heating and is dependent on the values of VIN, VOUT and case temperature. See Typical Performance Curves.

⑧ Continuous operation at or above absolute maximum ratings may adversely effect the device performance and/or life cycle.

⑨ Pre and post irradiation limits @ 25°C, up to 100 Krad TID, are identical unless otherwise specified. Post irradiation performance is guaranteed by design with a 2X radiation design margin.

## APPLICATION NOTES

### *PIN FUNCTIONS*

*VIN A,B,C,D,E* - These pins provide the input power connection to the MSK5950RH. This is the supply that will be regulated to the output. All five pins must be connected for proper operation.

*VBIAS* - This pin provides power to all internal circuitry including bias, start-up, thermal limit and overcurrent latch. VBIAS voltage range is 2.9V to 7.5V. VBIAS should be kept greater than or equal to VIN.

*VREF* - Internal general purpose 2.5V shunt regulator that will operate over a wide current range while maintaining good stability. This reference voltage is used along with the feedback voltage to configure the desired output voltage. The reference will maintain good regulation as long as $0.4 \leq I_{SHUNT} \leq 10mA$. The shunt current is derived from a resistor tied to VIN or VBIAS. The resistor must supply both the minimum shunt current of 400µA (1mA recommended) and the current required by the output voltage feedback divider network, between 2 and 2.5mA total is typically sufficient. A constant current diode (CCR) may be used in place of the resistor to minimize variations in $I_{SHUNT}$ due to line voltage variations.

Resistor calculation example:

VBIAS=3.3V±10%
VOUT=0.9V

First determine the required current by selecting R2 in the feed back divider, typically between 1.0 and 1.2KΩ; see the output voltage selection paragraph. Using standard value 0.1% tolerance resistors, the nominal output will be 0.9V with R2=1.07K and R1=316Ω. The current in the divider will be equal to $(V_{REF}-V_{FDBK}) / R2$ or 1.154mA nominal and 1.2mA worst-case in this example.

The total current required is the sum of the worst-case divider current plus the VREF shunt current. The minimum shunt current is 400µA but 1mA is recommended. Using the recommended 1mA the minimum current required in $R_{REF}$ is 2.2mA.

The maximum resistor value to source the required current is equal to (VBIAS min-VREF) / 2.2mA or 218Ω for this example. The maximum current in the reference must not exceed 10mA, the absolute maximum allowable bias voltage is $10mA*R_{REF}+VREF(min)$ or 4.67V for this application.

The designer must also consider that the feedback divider will provide a resistive connection from the source (VIN or VBIAS) to the output even when the regulator is disabled. A minimum load resistor can be used to draw the voltage down in the event this poses a problem. A 90Ω resistor will sink 10mA during operation and pull the output well below 200mV when the regulator is disabled in this application.

*VREF* can be used as a precision 2.5V reference for other parts of the circuit as long as circuit loading, shunt current and parasitics are carefully considered.

*GND1* - SIGNAL GROUND - Internally connected to the reference ground, these pins should be connected externally by the user to the circuit ground and the GND2 pins.

*VOUT A,B,C,D,E* - These are the output pins for the device. All five pins must be connected for proper operation.

*GND2* - POWER GROUND - Internally connected to the pass element drive circuitry, these pins should be connected externally by the user to the circuit ground and the GND1 pins.

*LATCH* **-** The MSK5950RH LATCH pin is used for both current limit and thermal limit. A capacitor between the LATCH pin and ground sets a time out delay in the event of an over current or short circuit condition. The capacitor is charged to approximately 1.6V from a 7.2µA (nominal) current source. Exceeding the thermal limit will charge the latch capacitor from a larger current source for a near instant shutdown. Once the latch capacitor is charged the device latches off until the latch is reset. Momentarily pull the LATCH pin low, toggle the shutdown pin high then low or cycle the power to reset the latch. Toggling the shutdown pin or cycling the bias power both disable the device during the reset operation (see SHUTDOWN pin description). Pulling the LATCH pin low immediately enables the device for as long as the LATCH pin is held low plus the time delay to re-charge the latch capacitor whether or not the fault has been corrected. Disable the latch feature by tying the LATCH pin low. With the LATCH pin held low the thermal limit feature is disabled and the current limit feature will force the output voltage to droop but remain active if excessive current is drawn.

*SHUTDOWN* **-** There are two functions to the SHUTDOWN pin. It may be used to disable the output voltage or to reset the LATCH pin. To activate the shutdown/reset functions the user must apply a voltage greater than 1.3V to the SHUTDOWN pin. The voltage applied to the SHUTDOWN pin can be greater than the input voltage. The output voltage will turn on when the SHUTDOWN pin is pulled below the threshold voltage. If the SHUTDOWN pin is not used, it should be connected to ground.

*FB* **-** The FB pin is the inverting input of the internal error amplifier. The non-inverting input is connected to an internal 1.265V reference. This error amplifier controls the drive to the output transistor to force the FB pin to 1.265V. An external resistor divider is connected to the output, FB pin, VREF and VIN to set the output voltage.

### *POWER SUPPLY BYPASSING*

To maximize transient response and minimize power supply transients it is recommended that a 33µF minimum tantalum capacitor is connected between VIN and ground. A 0.1µF ceramic capacitor should also be used for high frequency bypassing.

### *OUTPUT CAPACITOR SELECTION*

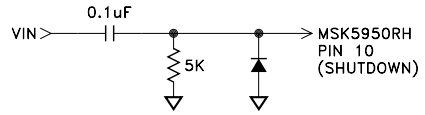
Low ESR output capacitors are required to maintain regulation and stability. Four CWR29FB227 (AVX PN TAZH227K010L) tantalum capacitors in parallel with ceramic decoupling capacitors (0.1µF typical) provides sufficient gain and phase margin for most applications. The maximum ESR specification for the CWR29FB227 capacitor is 180mΩ at 100kHz and is sufficient for many applications. It has been found through full WCCA on the MSK5820RH-1.5 that screening for a maximum ESR of 57mΩ ensures EOL stability criteria to be met for many applications with the most stringent requirements. Analysis of the final design is recommended to ensure stability requirements are met.

## *THERMAL LIMITING*

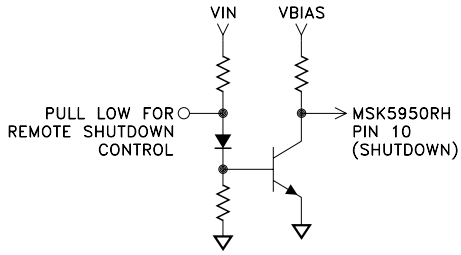
The MSK5950RH control circuitry has a thermal shutdown temperature of approximately 150°C. This thermal shutdown can be used as a protection feature, but for continuous operation, the junction temperature of the pass transistor must be maintained below 150°C. Proper heat sink selection is essential to maintain these conditions. Exceeding the thermal limit activates the latch feature of the MSK5950RH. See LATCH pin description for instructions to reset the latch or disable the latch feature.

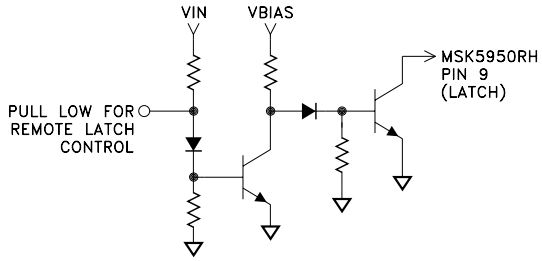
## *START UP OPTIONS*

The MSK5950RH starts up and begins regulating immediately when VBIAS and VIN are applied simultaneously. Applying VBIAS before VIN starts the MSK5950RH up in a disabled or latched state. When starting in a latched state the device output can be enabled either by pulling the latch pin low to drain the latch capacitor or pulsing the shutdown pin high. The shutdown pulse duration is partially dependent upon the size of the latch capacitor and should be characterized for each application; 30uS is typically adequate for a 1uF latch capacitor at 25°C. A momentary high pulse on the shutdown pin can be achieved using the RC circuit below if VIN rises rapidly. The resistor and capacitor must be selected based on the required pulse duration, the rise characteristic of VIN and the shutdown pin threshold (see shutdown pin threshold and current curves).




The shutdown pin can be held high and pulled low after VIN comes up or the latch pin held low and released after VIN comes up to ensure automatic startup when applying VBIAS before VIN. Either of the basic circuits below can be adapted to a variety of applications for automatic start up when VBIAS rises before VIN.




## *OVERCURRENT LATCH-OFF/LATCH PIN CAPACITOR SELECTION*

As previously mentioned, the LATCH pin provides over current/ output short circuit protection with a timed latch-off circuit. Reference the LATCH pin description note. The latch off time out is determined with an external capacitor connected from the LATCH pin to ground. The time-out period is equal to the time it takes to charge this external capacitor from 0V to 1.6V. The latch charging current is provided by an internal current source. This current is a function of bias voltage and temperature (see latch charging current curve). For instance, at 25°C, the latch charging current is 7.2µA at VBIAS = 3V and 8µA at VBIAS = 7V.

In the latch-off mode, some additional current will be drawn from the bias supply. This additional latching current is also a function of bias voltage and temperature (see typical performance curves).

The MSK5950RH current limit function is directly affected by the input and output voltages. Custom current limit is available; contact the factory for more information.

## *HEAT SINK SELECTION*

To select a heat sink for the MSK5950RH, the following formula for convective heat flow may be used.

*Governing Equation:*

$$T_J = P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$

Where

| | | |
|---|---|---|
| $T_J$ | = | Junction Temperature |
| $P_D$ | = | Total Power Dissipation |
| $R_{\theta JC}$ | = | Junction to Case Thermal Resistance |
| $R_{\theta CS}$ | = | Case to Heat Sink Thermal Resistance |
| $R_{\theta SA}$ | = | Heat Sink to Ambient Thermal Resistance |
| $T_A$ | = | Ambient Temperature |

$$\text{Power Dissipation} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Next, the user must select a maximum junction temperature. The absolute maximum allowable junction temperature is 150°C. The equation may now be rearranged to solve for the required heat sink to ambient thermal resistance ($R_{\theta SA}$).

*Example:*

An MSK5950RH is connected for $V_{IN}$ = +3.3V and $V_{OUT}$ = +1.2V. $I_{OUT}$ is a continuous 1A DC level. The ambient temperature is +25°C. The maximum desired junction temperature is +125°C.

$R_{\theta JC}$ = 8.4°C/W and $R_{\theta CS}$ = 0.15°C/W for most thermal greases

Power Dissipation = (3.3V - 1.2V) x (1A)

= 2.1Watts

Solve for $R_{\theta SA}$:

$$R_{\Theta SA} = \left[\frac{125°C - 25°C}{2.1W}\right] - 8.4°C/W - 0.15°C/W$$

$$= 39°C/W$$

In this example, a heat sink with a thermal resistance of no more than 39°C/W must be used to maintain a junction temperature of no more than 125°C.

## *START UP CURRENT*

The MSK5950RH sinks increased current during startup to bring up the output voltage. Reference the "Saturated Drive Current vs. Input Voltage" graph in the typical performance curves of this data sheet and the "Understanding Startup Surge Current With RH1573 Based Rad Hard LDO Regulators" application note in the application notes section of the TTM Technologies Web site for more information.

## *TOTAL DOSE RADIATION TEST PERFORMANCE*

Radiation performance curves for TID testing have been generated for all radiation testing performed by TTM Technologies. These curves show performance trends throughout the TID test process and are located in the MSK5950RH radiation test report. The complete radiation test report is available in the RAD HARD PRODUCTS section on the TTM Technologies website.

## *TYPICAL APPLICATIONS CIRCUIT*

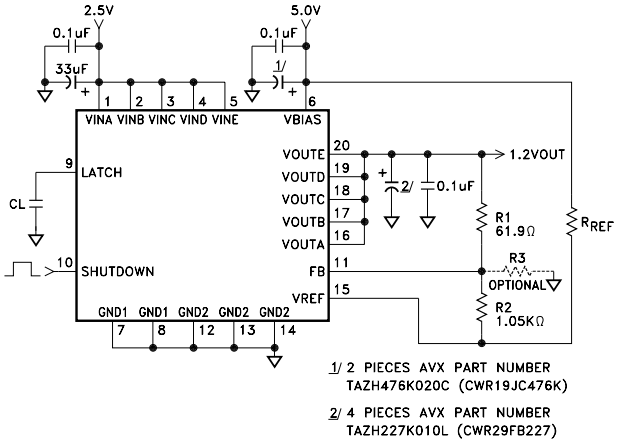



FIGURE 1

## *OUTPUT VOLTAGE SELECTION*

The MSK5950RH output voltage can be adjusted from 0 to 5V. Three different resistor network schemes are used depending on the required output voltage level.

For output voltages below the minimum feedback voltage tolerance of 1.225V, R3 as shown in Figure 1 can be omitted. Output voltage can be calculated as follows:

Given:
$V_{FB}$ = 1.265V
VREF = 2.5V

VOUT = $V_{FB}$ - ((VREF - $V_{FB}$)/R2) R1

For convenience Table 1 below provides standard 0.1% tolerance resistor values required to achieve several output voltages based on nominal feedback voltage, R3 is ommitted.

| OUTPUT VOLTAGE (V) | R2 (Ω) | R1 (Ω) |
|---|---|---|
| 1.10 | 1.01K | 135 |
| 1.05 | 1.00K | 174 |
| 1.00 | 1.00K | 215 |
| 0.95 | 1.00K | 255 |
| 0.90 | 1.07K | 316 |
| 0.85 | 1.00K | 336 |
| 0.80 | 1.04K | 392 |
| 0.75 | 1.00K | 417 |
| 0.70 | 1.09K | 499 |
| 0.65 | 1.05K | 523 |
| 0.60 | 1.02K | 549 |
| 0.55 | 1.07K | 619 |
| 0.50 | 1.14K | 706 |

For output voltages close to the feedback voltage tolerance of 1.225V - 1.305V, a three resistor network may be used to improve adjustment capabilities and trim out initial feedback voltage tolerances. Reference Figure 1.

VOUT = (R2R3$V_{FB}$ + R1R3 ($V_{FB}$ - VREF) + R1R2$V_{FB}$) / (R2R3)

## APPLICATION NOTES CONT'D

For output voltages above the feedback voltage the unit should be configured as shown in Figure 2.

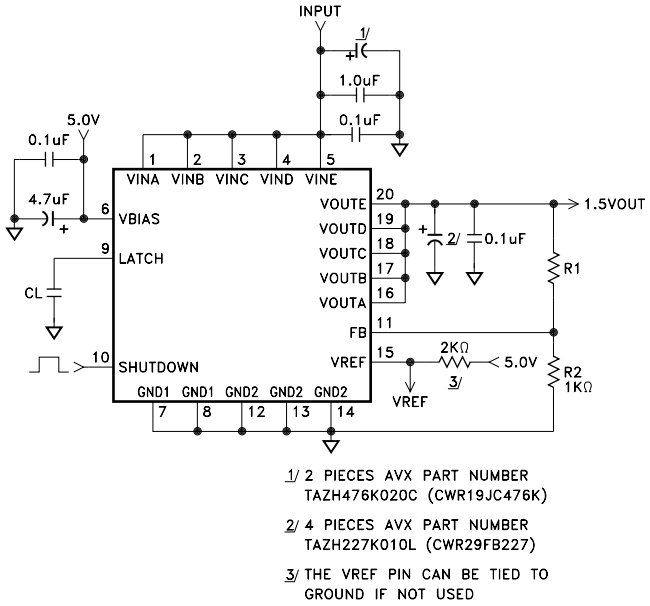



FIGURE 2

VOUT = 1.265 (1 + R1/R2)

As noted in the above typical applications circuit, the formula for output voltage selection is:

VOUT = 1.265 (1 + (R1/R2))

A good starting point for this output voltage selection is set to R2 = 1K. By rearranging the formula it is simple to calculate the final R1 value.

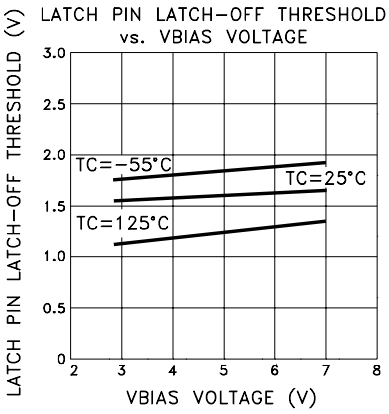
R1 = R2 ((VOUT/1.265) -1)

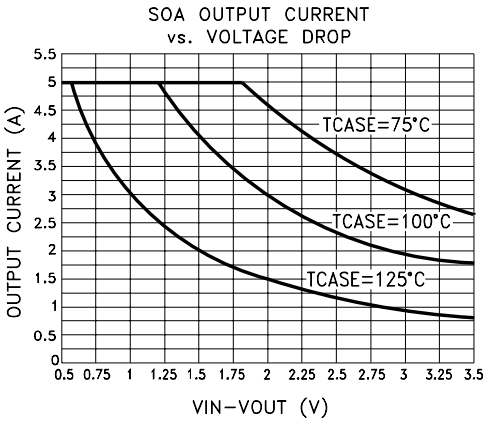
Table 3 below lists some of the most probable resistor combinations based on industry standard usage, R3 is ommitted.

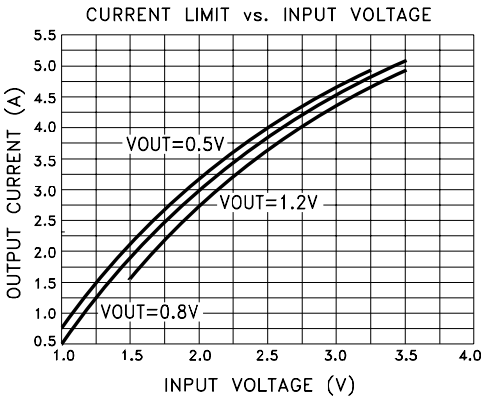
| OUTPUT VOLTAGE (V) | R2 (Ω) | R1 (Ω) |
|---|---|---|
| 1.5 | 1K | 187 |
| 1.8 | 1K | 422 |
| 2.0 | 1K | 576 |
| 2.5 | 1K | 976 |
| 2.5 | 1K | 1.21K |
| 3.3 | 1K | 1.62K |
| 4.0 | 1K | 2.15K |
| 5.0 | 1K | 2.94K |

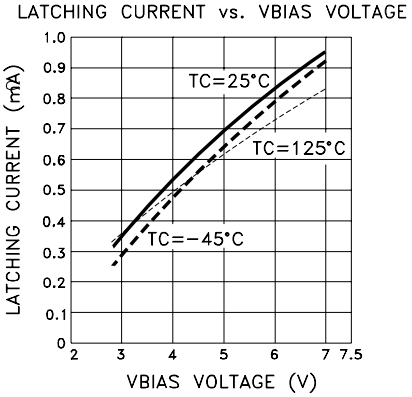
VREFcan be used as a precision 2.5V reference as long as circuit loading and shunt current are carefully considered. If VREF is not used the pin should be pulled to ground.

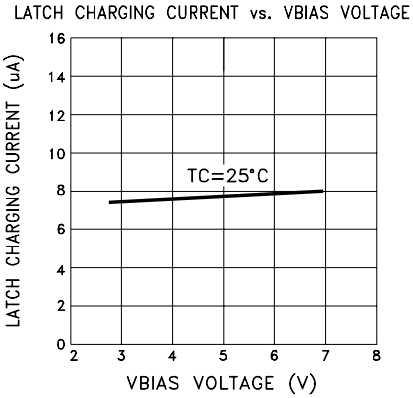
## TYPICAL PERFORMANCE CURVES

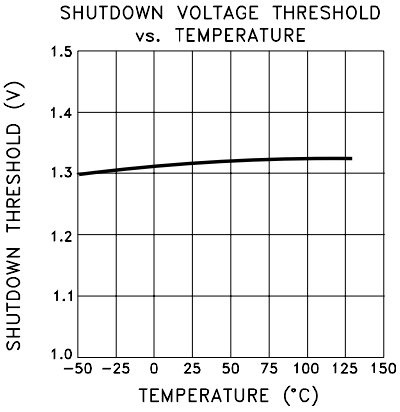


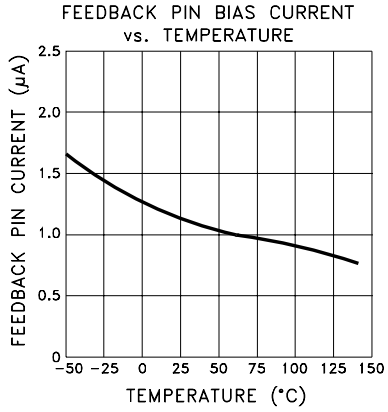



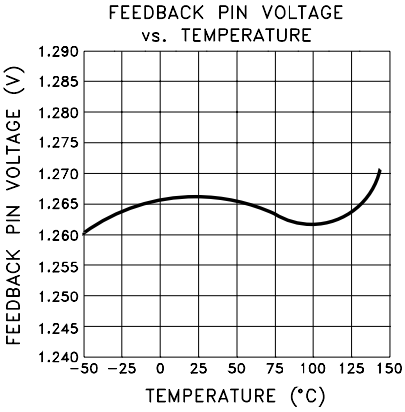



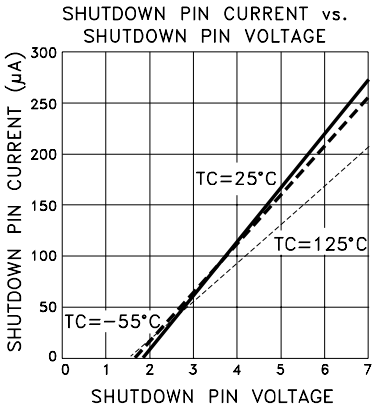



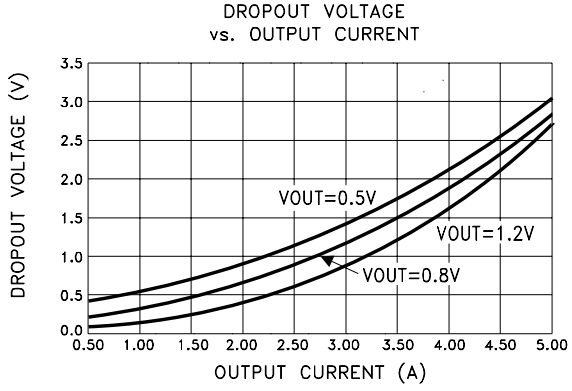



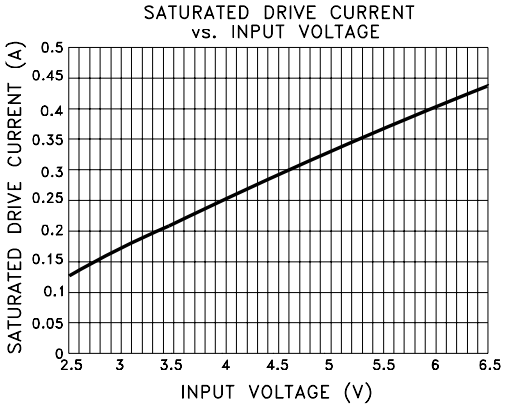



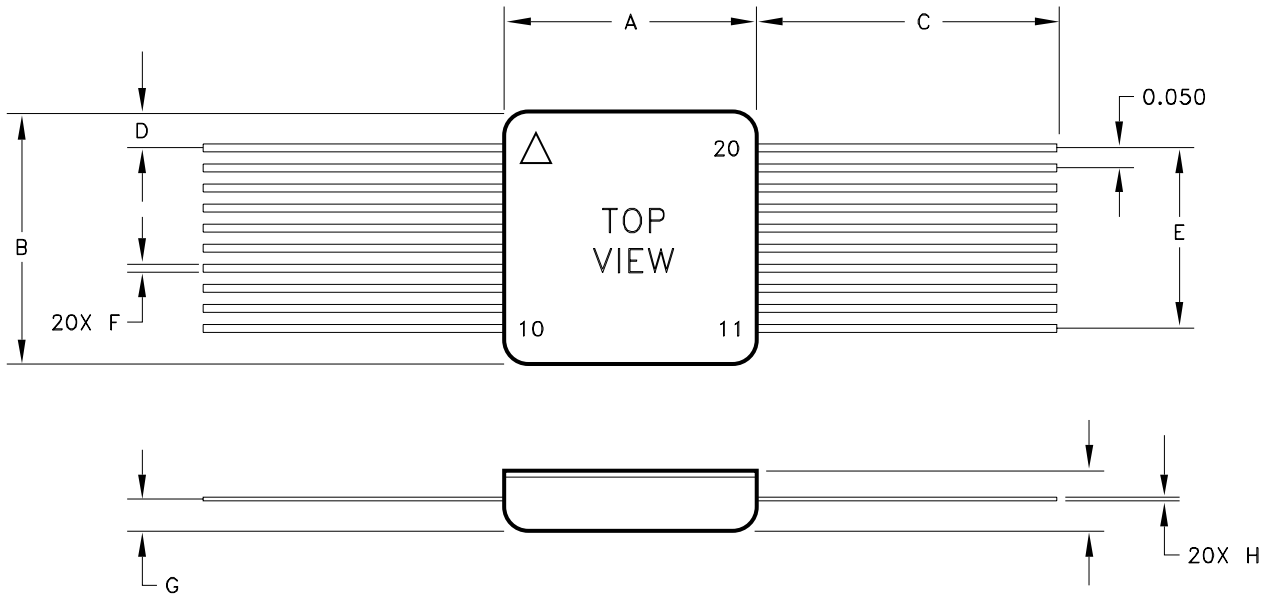



## MECHANICAL SPECIFICATIONS




| REF | MIN | MAX |
|---|---|---|
| A | 0.620 | 0.630 |
| B | 0.620 | 0.630 |
| C | 0.500 | ——— |
| D | 0.087 REF. | |
| E | 0.445 | 0.455 |
| F | 0.013 | 0.017 |
| G | 0.076 | 0.086 |
| H | 0.008 | 0.012 |
| I | 0.145 | 0.155 |

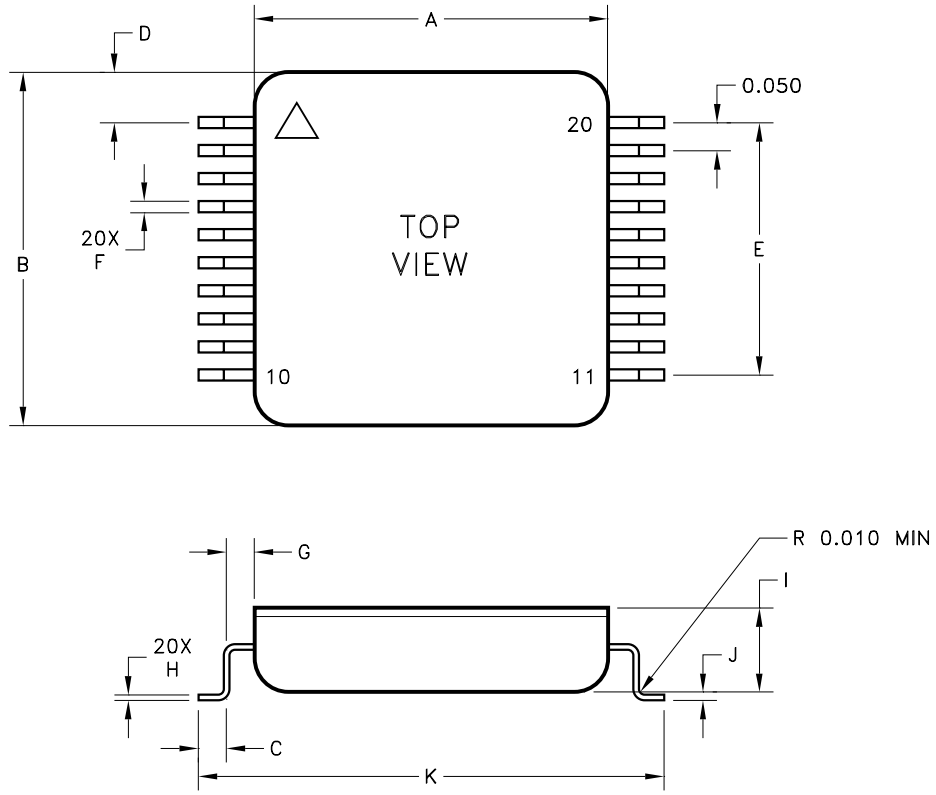
ESD TRIANGLE INDICATES PIN 1
WEIGHT = 3.5 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

# *ORDERING INFORMATION*

| PART NUMBER | SCREENING LEVEL | LEADS |
|---|---|---|
| MSK5950RH | INDUSTRIAL | STRAIGHT |
| MSK5950HRH | MIL-PRF-38534 CLASS H | |
| MSK5950KRH | MIL-PRF-38534 CLASS K | |

## MECHANICAL SPECIFICATIONS CONT'D




| REF | MIN | MAX |
|---|---|---|
| A | 0.620 | 0.630 |
| B | 0.620 | 0.630 |
| C | 0.045 | 0.055 |
| D | 0.087 REF. | |
| E | 0.445 | 0.455 |
| F | 0.013 | 0.018 |
| G | 0.045 | 0.055 |
| H | 0.008 | 0.012 |
| I | ——— | 0.155 |
| J | 0.008 | 0.018 |
| K | 0.805 | 0.845 |

ESD TRIANGLE INDICATES PIN 1
WEIGHT = 3.3 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

# *ORDERING INFORMATION*

| PART NUMBER | SCREENING LEVEL | LEADS |
|---|---|---|
| MSK5950RHG | INDUSTRIAL | GULL WING |
| MSK5950HRHG | MIL-PRF-38534 CLASS H | |
| MSK5950KRHG | MIL-PRF-38534 CLASS K | |

## REVISION HISTORY

| REV | STATUS | DATE | DESCRIPTION |
|---|---|---|---|
| H | Released | 01/14 | Update IQ specifications and test methods to match MSK5810 and test VREF seperately.<br>Clarify figure 2 by adding note 3.<br>Delete incomplete performance curves on original sheet 7. |
| I | Released | 04/14 | Update bias supply voltage, feedback voltage and output voltage range specifications. |
| J | Released | 06/14 | Add maximum rating for shutdown input. |
| K | Released | 04/16 | Remove note 10 on page 2. |
| L | Released | 07/17 | Change standard TID hardness to 100 Krads(Si).<br>Add Post RAD VREF Load REG Limit |
| M | Released | 09/17 | Update parameters to better correlate to manufacturer's pre and post RAD specs. |
| N | Released | 04/22 | Remove MIL-PRF-38535, update company name and website |



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