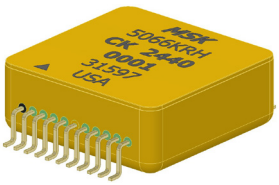
MIL-PRF-38534 CERTIFIED FACILITY

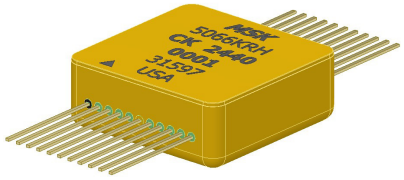
RAD HARD 3A SWITCHING REGULATOR

5066RH

TTM Technologies
Time-To-Market Interconnect Solutions

FEATURES:



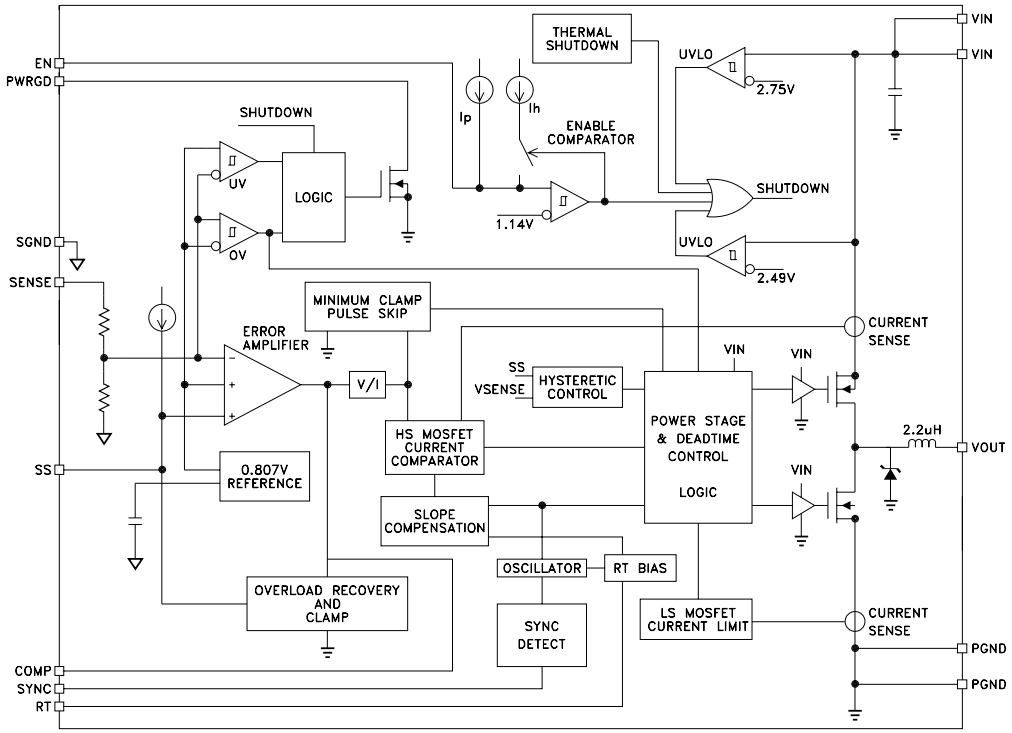


- Total Dose Hardened to 100 kRAD(Si)
- SEL, SEB, and SEGR immune to LET of 75 MeV-cm^2/mg
- Precision Trimmed Output Voltages: 0.9V, 1.0V, 1.1V, 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V
- Input Voltage Range from 3.0V to 5.5V
- Overvoltage and Undervoltage Lockout, Power Good Monitor
- Enable and Soft Start Inputs
- MIL-PRF-38534 Class H & K Processing & Screening
- Contact TTM Technologies for MIL-PRF-38534 Qualification Status
- Custom trim set points available by request

DESCRIPTION:

The MSK5066RH is a 3A radiation hardened buck switching regulator with precision trimmed output voltage. The regulator design uses peak current mode control and features an integrated inductor, feedback network, and power MOSFETs. The regulator operates at a user programmable or synchronized fixed frequency, and features cycle by cycle current limiting. The device is packaged in a hermetically sealed 22 pin flatpack, available with straight or gull wing leads.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Point of Load Regulation
- Microprocessor/FPGA Power Supply
- RF Amplifier Supply

PIN-OUT INFORMATION

1	EN	7	VIN	13	VOUT	19	SGND
2	RT	8	PGND	14	VOUT	20	COMP
3	SYNC	9	PGND	15	VOUT	21	SS
4	VIN	10	PGND	16	VOUT	22	PWRGD
5	VIN	11	PGND	17	CASE		
6	VIN	12	VOUT	18	SENSE		

ABSOLUTE MAXIMUM RATINGS (4)

VIN, SYNC	PGND -0.3V TO +7.5V
SGND	PGND ±0.2V
EN, PG, SS, TR, RT	PGND -0.3 TO PGND +5.5V
COMP	PGND -0.3 TO 3.3V
RT	±100µA
COMP	±200µA
PG	-0.1 to 5mA

Storage Temperature range	-65 to 150°C
Lead Temperature Range	300°C
Case Operating Temperature Range	-55°C to 125°C
Junction Temperature	150°C
ESD Rating	±750V
(HBM per ANSI/ESDA/JEDEC JS-001, all pins)	

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions (1) (2)	Group A Subgroup	MSK 5066K/H/RH Min.	Typ.	Max.	Units
RISING EDGE UVLO (5)	ENABLE = 1.18V	1, 2, 3		2.5		V
BIAS CURRENT, NON-SWITCHING	VIN = 3V, ENABLE = 1.18V	1, 2, 3		2.5	5.0	mA
STANDBY BIAS CURRENT	VIN = 3V, ENABLE = 0V	1, 2, 3		1.75	3.0	mA
VOUT TOLERANCE	VIN = 5V	1, 2, 3	-1	-	+1	%
LINE REGULATION		1, 2, 3		0.0	0.5	%
LOAD REGULATION		1, 2, 3		0.05	0.5	%
POSITIVE PEAK CURRENT LIMIT (5)	VIN = 3V	1, 2, 3		7.9		A
	VIN = 5.5V	1, 2, 3		6.2		A
NEGATIVE PEAK CURRENT LIMIT (5)	VIN = 5V	1, 2, 3		8		A
OUTPUT CURRENT LIMIT		1, 2, 3		TBD		A
THERMAL SHUTDOWN (5)		-		170		°C
THERMAL SHUTDOWN HYSTERESIS (5)		-		30		°C
ERROR AMP TRANSCONDUCTANCE (5)		1, 2, 3		1.4		mA/V
ERROR AMP GAIN (5)		1, 2, 3		80		dB
INTERNALLY SET FREQUENCY	RT = OPEN	4, 5, 6	395	500	585	KHz
EXTERNALLY SET FREQUENCY	RT = 100KΩ (1%)	4, 5, 6	395	500	585	KHz
	RT = 487KΩ (1%)	4, 5, 6	80	100	115	KHz
	RT = 47KΩ (1%)	4, 5, 6	900	1000	1100	KHz
SLOPE COMP (5)	100KHz	4, 5, 6		-0.69		A/µS
	500KHz	4, 5, 6		-3.4		A/µS
	1MHz	4, 5, 6		-7		A/µS
RISING EDGE ENABLE	ENABLE RISING EDGE TO VOUT = 10%	1, 2, 3		1.14	1.18	V
FALLING EDGE ENABLE	ENABLE FALLING EDGE TO VOUT = 90%	1, 2, 3	1.05	1.12		V
OUTPUT OVERVOLTAGE ERROR THRESHOLD (5)	FB AS % OF VREF	1, 2, 3		106		%
OUTPUT UNDERVOLTAGE ERROR THRESHOLD (5)	FB AS % OF VREF	1, 2, 3		94		%
OUTPUT OVERVOLTAGE FAULT (5)	FB AS % OF VREF	1, 2, 3		109		%
OUTPUT UNDERVOLTAGE FAULT (5)	FB AS % OF VREF	1, 2, 3		91		%
THERMAL RESISTANCE	(AVERAGE THERMAL RESISTANCE ACROSS ENTIRE DIE)	-	-	10.2	10.3	°C/W
EFFICIENCY		1, 2, 3		TBD	-	%

NOTES:

(1) Unless otherwise indicated, VIN = 3.3V, FSW = 500KHz (internally set), Slope Comp = -3.4 A/µS, I_{OUT} = 1.5A

(2) Military grade devices shall be 100% screened to subgroup 1-6.
Subgroup 1, 4 $T_A = T_C$ = +25°C
Subgroup 2, 5 $T_A = T_C$ = +125°C
Subgroup 3, 6 $T_A = T_C$ = -55°C

(3) Industrial grade devices shall be 100% screened to Subgroup 1 & 4.

(4) Operation at or above Absolute Maximum Ratings may adversely affect performance and service life.

(5) Guaranteed by design. Typical parameters are representative of actual device performance but are for reference only.

(6) Internal Solder reflow temperature is 220°C, Do Not Exceed.

(7) Pre and Post Irradiation Limits at 25°C up to 100kRAD(Si) TID limits are identical unless otherwise specified.

TABLE 1 PIN LIST

Name	Pin	Unit
EN	1	The EN pin serves as the Enable input. When EN is less than 1.18V the device is in shutdown mode, drawing a maximum current of 3.0mA. EN Pin has internal pull-up. EN Pin needs to be actively held low to be disabled. The EN voltage can be scaled down to create an undervoltage lockout.
RT	2	Float pin to set internal oscillator to 500kHz, or connect timing resistor to set oscillator externally.
SYNC	3	Internal Oscillator Mode configure by connecting resistor from RT to SGND, connect 10kΩ from SYNC to SGND. RT resistor must be between 47kΩ and 510kΩ, calculated as follows: $RT=67009 \cdot F_{SW}{}^{-1.0549}$:, enter F_{SW} as kHz and RT will be in kΩ. External Clock Mode configure by connecting resistor from RT to SGND. RT resistor must be between 47kΩ and 510kΩ, calculated as follows: $RT = 67009 \cdot F_{SW}{}^{-1.0549}$:, enter F_{SW} as kHz and RT will be in kΩ. The module will monitor the SYNC pin for an external clock and the switching frequency will be set by the external synchronization pulses. If no SYNC pulse is received for 20µs, then the module will operate with F_{SW} = 500kHz.
VIN	4	The VIN pins are the power and control inputs to the module. High di/dt switching currents are conducted through these pins. Locally decouple to PGND using both ceramic and low ESR tantalum capacitors. Provide sufficient bulk capacitance to limit input ripple and ensure a low impedance input supply.
VIN	5	
VIN	6	
VIN	7	
PGND	8	The PGND pins are the high-current ground reference. Connect directly to negative side of VIN decoupling capacitors. High di/dt switching currents are conducted through these pins. Provide a continuous low impedance ground path between the PGND pins, the input supply return and the load. Avoid layouts that force the load return current to cross the SGND reference path.
PGND	9	
PGND	10	
PGND	11	
VOUT	12	The VOUT pins provide access to the output of the regulator. External capacitance is required to maintain stability.
VOUT	13	
VOUT	14	
VOUT	15	
VOUT	16	
CASE	17	The CASE pin provides electrical connection to the package. The package and CASE pin are isolated from all internal circuitry.
SENSE	18	The regulator has an internal divider that is laser trimmed to achieve the required output voltage. This pin must connect to VOUT for proper operation and to avoid damage to the module.
SGND	19	The SGND pin provides a low noise signal reference for internal control circuitry. Connect to PGND as close to the ground side of the load as practical.
COMP	20	The COMP pin provides access to the output of the error amplifier to allow for frequency compensation.
SS	21	Connect external capacitor between SS pin and SGND to set the internal voltage reference rise time. Bottom FET is held off, until the voltage at SS pin reaches 1.55V. Soft Start time is calculated as $t\_SS=(C\_SS \cdot V\_REF)/I\_SS$ where t_{SS} is in ms, C_{SS} is in nF, V_{REF} is in Volts, and I_{SS} is 2.5uA. Turn-on after fault will not begin until SS pin reaches 0V.
PWRGD	22	The PWRGD pin is an output of the internal control circuitry. The pin is pulled low if VOUT falls outside 91% to 109% of VREF. PWRGD Pin will also be low in the event of thermal shutdown, EN shutdown and soft start. Normal operation when VSENSE is between 94% to 106% of VREF. Pull up resistor should be between 10kΩ to 100kΩ with a pull-up voltage not to exceed 5.5V.

APPLICATION NOTES

SELECTING THE INPUT CAPACITOR

The input capacitors minimize the source impedance by providing a low AC impedance local decoupling to the regulator. Select the input capacitors based on RMS current handling and maximum voltage rating. The input ripple current for a buck converter is high, typically IOUT/2. Tantalum capacitors become resistive at higher frequencies, requiring careful ripple-rating selection to prevent excessive heating. Use ceramic capacitor to handle high frequency switch transitions. Place ceramic input capacitors as close to the PGND and VIN pins as possible. Place tantalum input capacitors next to the ceramic. Ceramic capacitors help reduce high frequency conducted EMI.

ADJUSTABLE SWITCHING FREQUENCY

When using Internal Oscillator Mode connect a 10kΩ resistor from the SYNC pin to SGND. Then select a resistor from within the range of 47kΩ to 510kΩ to connect between the RT pin and SGND. The frequency may be computed using the following formula:

*RT(in kΩ) = 67009 * F_{SW}-1.0549, where F_{SW} is in kHz*

SELECTING THE OUTPUT CAPACITOR

The output capacitor filters the ripple current from the inductor to an acceptable ripple voltage seen by the load. The primary factor in determining voltage ripple is the ESR of the output capacitor. The required ESR can be calculated as:

$$R_{ESR} < \frac{V_{out\_ripple}}{I_{ripple}}$$

The output capacitance to meet a given ripple voltage can be calculated as:

$$C_{out} < \frac{I_{ripple}}{8 * F_{SW} * V_{out\_ripple}}$$

Select a capacitor or combination of capacitors that can tolerate the worst-case ripple current with sufficient de-rating. When using multiple capacitors in parallel to achieve ESR and/or total capacitance sharing of ripple current between capacitors will be approximately equal if all of the capacitors are the same type and preferably from the same lot. TTM recommends that low ESR tantalum capacitors be used as output capacitors whenever possible. The zero created by the ESR of the capacitor is necessary for loop stability. A small amount of ceramic capacitance close to the load to decouple high frequency is acceptable but it should not cancel the ESR zero.

LOOP COMPENSATION

The loop response can be adjusted via an external combined pole-zero-pole compensation network connected to the COMP pin.

Initial compensation values can be selected as follows:

- Set crossover frequency as Switching Frequency divided by 10

- Calculate:

$$R_3 = \frac{2\pi * F_{CO} * V_{OUT} * C_{OUT}}{(gm_{EA} = 0.0014S) * V_{REF} * (gm_{PS} = 12S)}$$

- Calculate:

$$C_1 = \frac{C_{OUT} * R_L}{R_3}$$

- Finally:

$$C_2 = \frac{C_{OUT} * R_{ESR}}{R_3}$$

Slope Compensation is internally controlled and is internally adjusted based on switching frequency.

ENABLE

When the EN pin exceeds 1.18V the device is enabled.

When the EN pin is less than 1.05V the device stops switching and draws less than 5mA. The EN pin has an internal pullup current source, so the pin may be floated for applications that require the supply to be always on.

For all other applications use open-drain or open-collector logic to interface with the EN pin.

UNDER VOLTAGE LOCK OUT

VIN has an UVLO of 3.0V with a typical hysteresis of 150 mV.

A resistive divider from VIN to EN can be used to set a programmable UVLO, calculate resistor values as follows:

$$R_{top} = \frac{V_{on} * \frac{1.12V}{1.14V} - V_{off}}{6.1\mu A \left(1 - \frac{1.12V}{1.14V}\right) + 3\mu A}$$

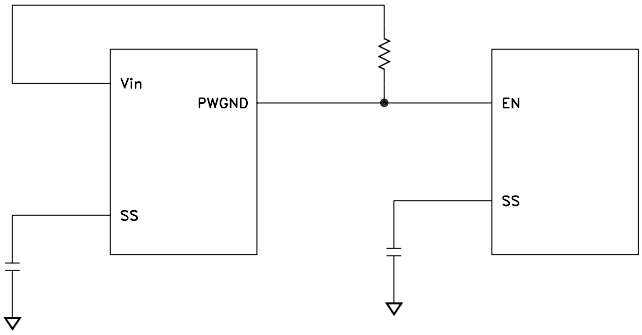
$$R_{bot} = \frac{R_{top} + 1.12V}{(V_{off} - 1.12V) + R_{top}\,(6.1\mu A + 3\mu A)}$$

APPLICATION NOTES CONT'D

SEQUENCING

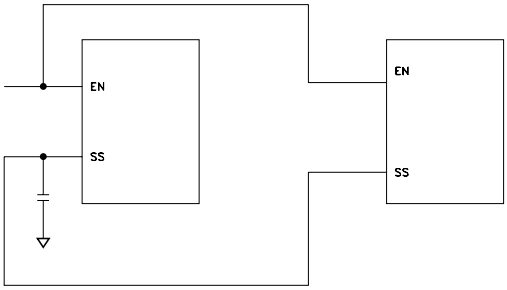
The device supports three options for startup, shown below.

Sequential Startup

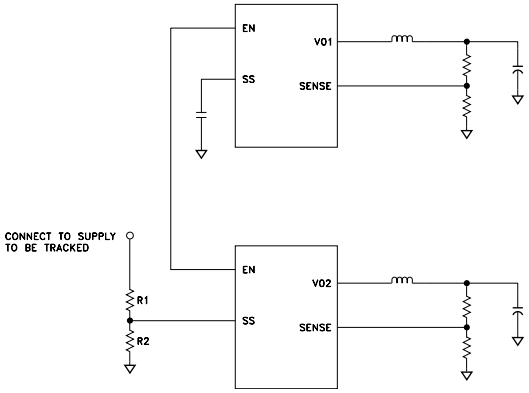


Ratiometric Startup

Note: Pullup current ISS is doubled in this configuration.



Ratiometric and Simultaneous Startup



$$R_1 = \frac{V_{OUT2} + \Delta V}{V_{Ref}} \bullet \frac{V_{ss} - Offset}{I_{SS}}$$

$$R_2 = \frac{V_{Ref} * R_1}{V_{OUT2} + \Delta V - V_{Ref}}$$

$\Delta V = V_{OUT1} - V_{OUT2}$; *set to 0 for simultaneous startup*

$$R_{1(min)} > 2800 \text{ X } V_{OUT1} - 180 \bullet \Delta V$$

$$R_1 > R_{1(min)}$$

SENSE

The sense resistors are precision resistors, trimmed to program the required output voltage within the specified tolerance.

The SENSE pin should be connected to the physical place on the PWB where the regulated voltage is required (no additional resistors are required). If desired, the voltage can be adjusted up by connecting a resistor in series with the sense line.

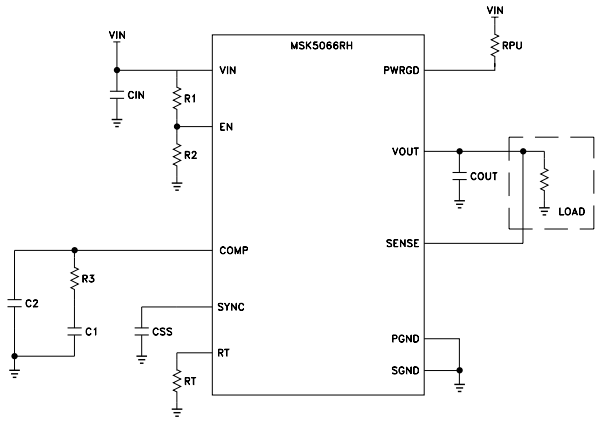
PREBIASED OUTPUTS

The low-side MOSFET is held off until the SS pin is greater than 1.55V, thereby preventing the low-side MOSFET from from discharging a prebiased output during monotonic startup.

STABILITY

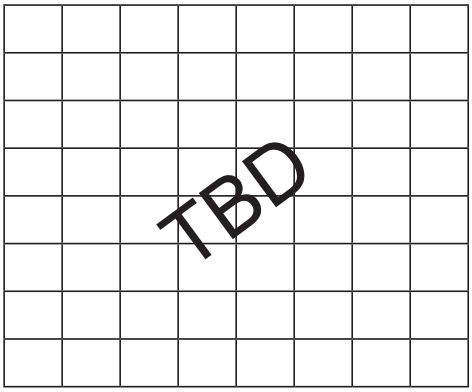
The stability of the device can be measured by inserting a small series resistance in the sense line and injecting a test signal across the resistor, sweeping the frequency and recording the results using any suitable VNA

Typical Application Circuit

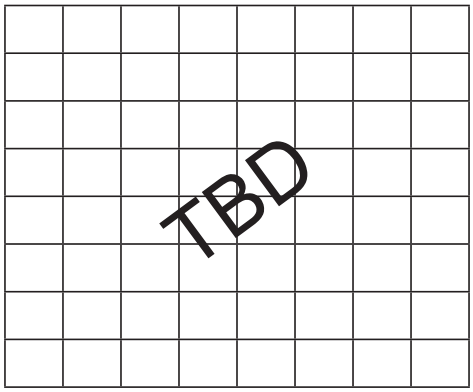


TYPICAL PERFORMANCE CURVES

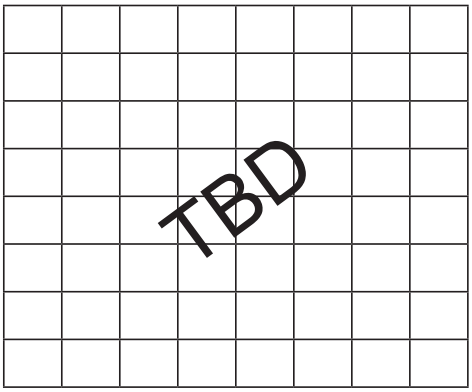
Supply Current vs Temperature



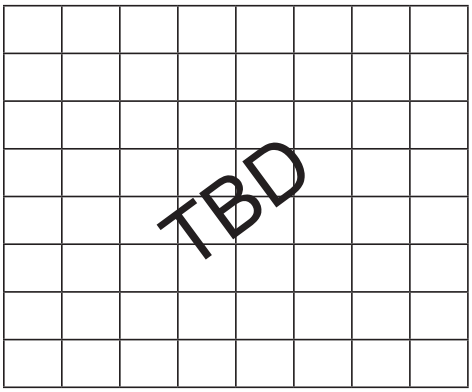
Switching Frequency vs Temperature



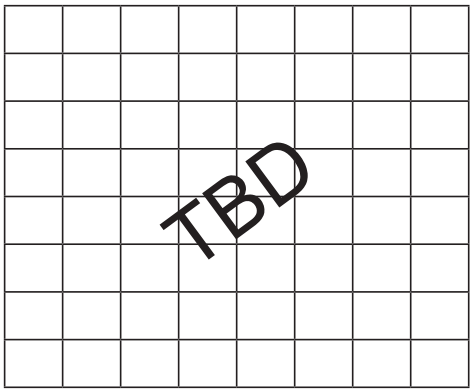
Enable Voltage vs Temperature



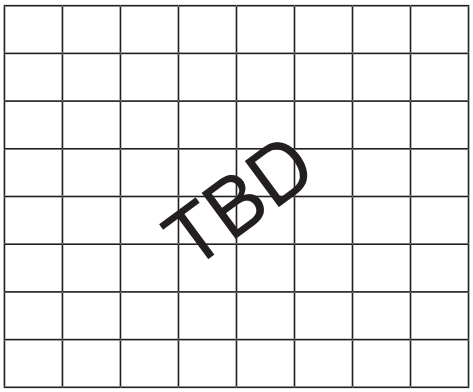
UVLO vs Temperature



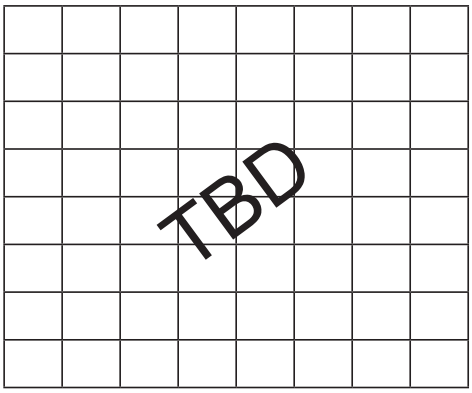
FB Leakage Current vs Temperature



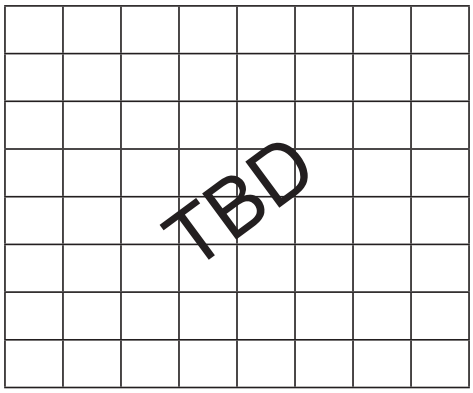
Minimum On/Off Time vs Temperature



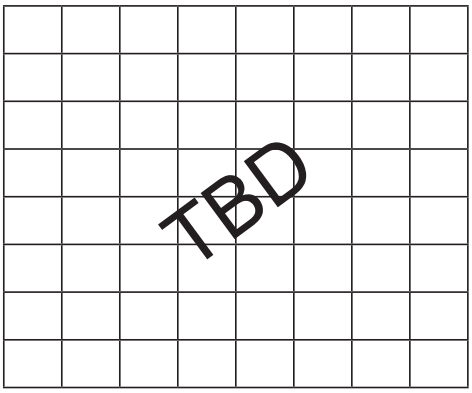
Soft Start Time vs Temperature



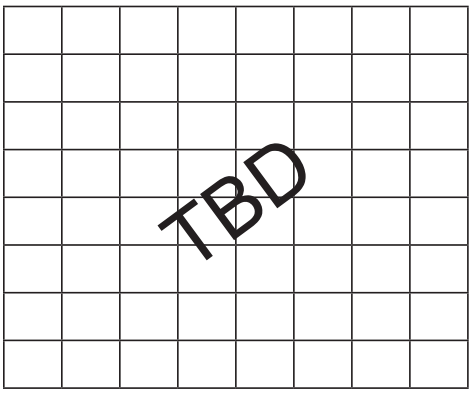
Positive Overcurrent Limit



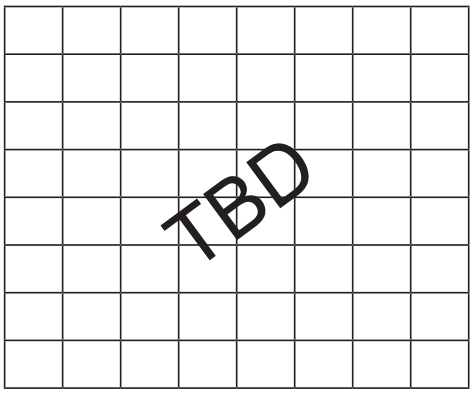
Negative Overcurrent Limit



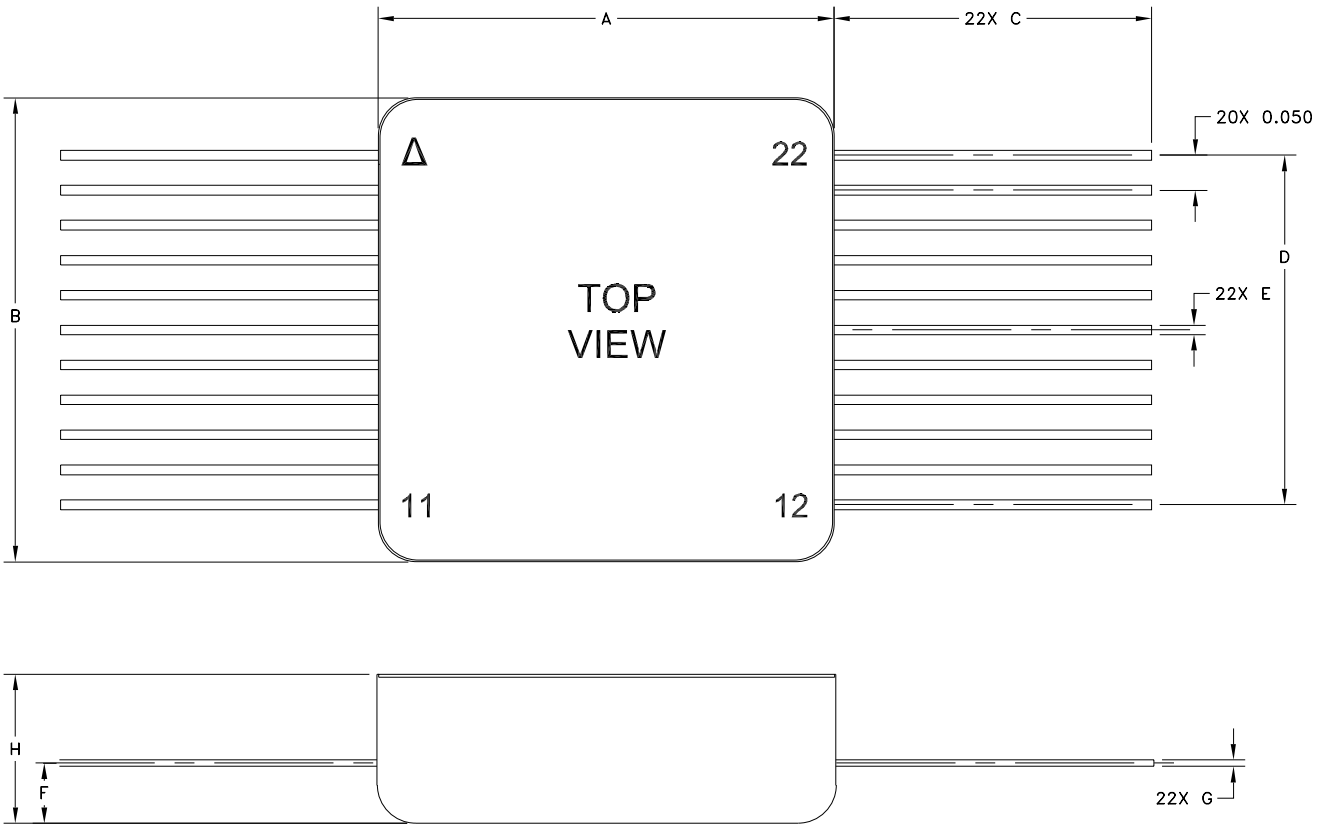
Gain and Phase vs Frequency



Efficiency vs Load Current



MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.707	0.727
B	0.720	0.740
C	0.500	———
D	0.495	0.505
E	0.012	0.018
F	0.112	0.127
G	0.008	0.012
H	———	0.275

ESD TRIANGLE INDICATES PIN 1
WEIGHT=0.36 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

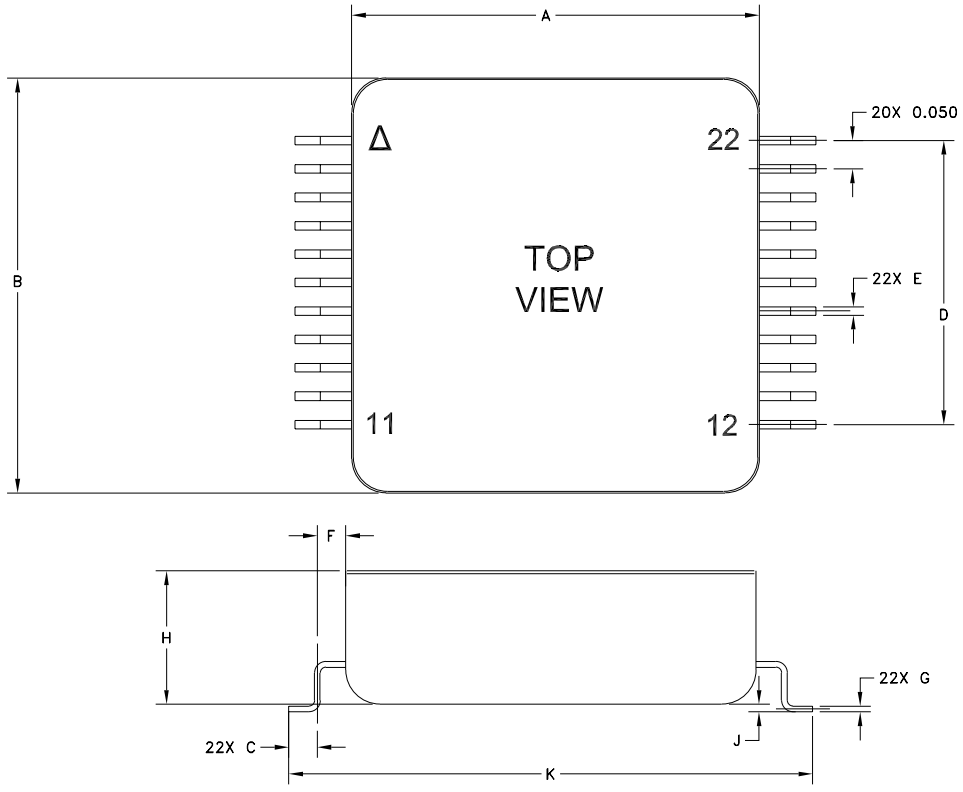
ORDERING INFORMATION

MSK5066-3.3 K RH

LEAD STYLE
BLANK = STRAIGHT
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL
H = MIL-PRF-38534 CLASS H
K = MIL-PRF-38534 CLASS K
OUTPUT VOLTAGE
1.0 = 1.0V; 1.1 = 1.1V; 1.2 = 1.2V; 1.5 = 1.5V; 1.8 = 1.8V;
2.5 = 2.5V; 3.3 = 3.3V
GENERAL PART NUMBER

The above example is a 3.3V, Class K reguator with straight leads.

MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.707	0.727
B	0.720	0.740
C	0.045	0.055
D	0.495	0.505
E	0.012	0.018
F	0.050 REF	
G	0.008	0.012
H	———	0.275
J	0.009	0.018
K	0.897	0.937

NOTE: DIMENSION "J" IS MEASURED FROM BOTTOM OF PIN TO BOTTOM OF CASE

ESD TRIANGLE INDICATES PIN 1
WEIGHT=0.36 GRAMS TYPICAL

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5066-3.3 K RH G

LEAD STYLE
G = GULL WING
RADIATION HARDENED
SCREENING
BLANK = INDUSTRIAL
H = MIL-PRF-38534 CLASS H
K = MIL-PRF-38534 CLASS K
OUTPUT VOLTAGE
1.0 = 1.0V; 1.1 = 1.1V; 1.2 = 1.2V; 1.5 = 1.5V; 1.8 = 1.8V;
2.5 = 2.5V; 3.3 = 3.3V
GENERAL PART NUMBER

The above example is a 3.3V, Class K reguator with gull wing leads.

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
A	Preliminary		Initial Release