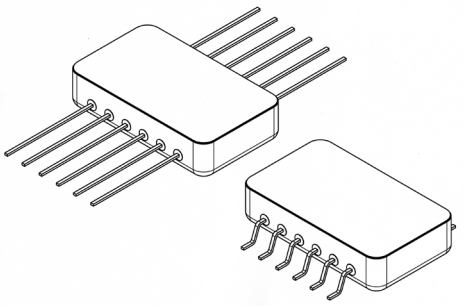
MIL-PRF-38534 CERTIFIED FACILITY

TTM Technologies
Time-To-Market Interconnect Solutions

RAD HARD 3A SWITCHING REGULATOR

5065RH

FEATURES:

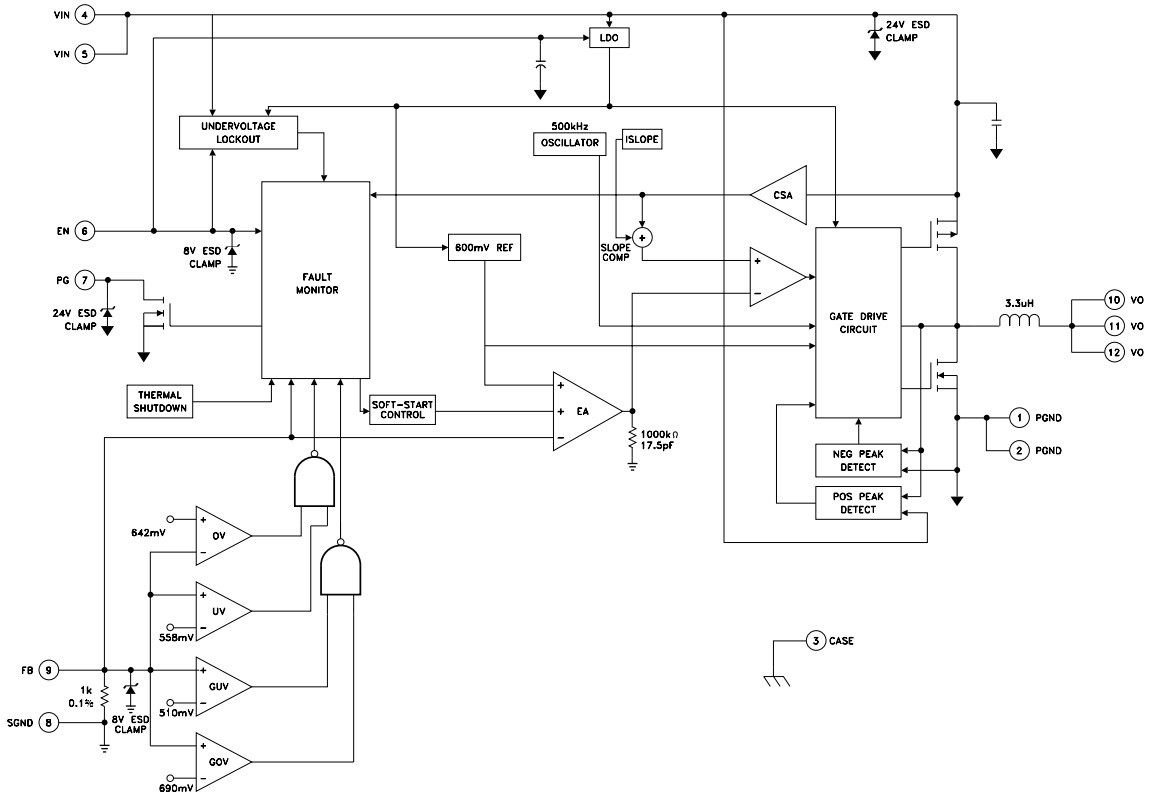


- Radiation Hardened to 100KRAD(Si) (target)
- Single Event Burnout free to Linear Energy Transfer of 86 MeV-cm²/(mg)
- Integrated inductor, Single Resistor Programmable Output Voltage
- Input Voltage Range from 3.0V to 16V
- Minimum Output Voltage 0.6V
- Constant 500kHz Switching Frequency
- Under Voltage Lock Out, Over Current Protection, Over Temperature Protection
- Soft Start, Power Good and Enable pins
- Typical Efficiencies exceed 85%

DESCRIPTION:

The MSK5065RH is a radiation hardened adjustable output switching buck regulator. The regulator design uses a 500kHz constant switching frequency with peak current mode control. The regulator features a Transconductance Error Amplifier with an integrated Error Amp compensation network in addition to an integrated slope compensation network. The device is packaged in a hermetically sealed 12 pin flatpack, available with straight or gull wing leads.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Point of Load Regulation
- Microprocessor/FPGA Power Supplies
- Step Down Synchronous Regulators
- Satellite System Power Supply

PIN-OUT INFORMATION

1	PGND	12	VOUT
2	PGND	11	VOUT
3	CASE	10	VOUT
4	VIN	9	FB
5	VIN	8	SGND
6	EN	7	PG

ABSOLUTE MAXIMUM RATINGS

VIN.....PGND-0.3V to PGND+16.5V
SGND .....PGND ±0.1V
EN, FB .....PGND -0.3V to PGND +5V
PG ..... PGND-0.3V to VIN

STORAGE TEMPERATURE RANGE (3) ..... -65°C to 150°C
LEAD TEMPERATURE RANGE .....300°C
JUNCTION TEMPERATURE .....150°C
CASE OPERATING TEMPERATURE.....125°C
ESD RATING..... 2

ELECTRICAL SPECIFICATIONS (4)

Parameter	Test Conditions (1)	Group A Subgroup	MSK 5065K/H/RH Min.	Typ.	Max.	Units
RISING EDGE UVLO	ENABLE = 2.25V	1, 2, 3			2.95	V
FALLING EDGE UVLO	ENABLE = 2.25V	1, 2, 3	2.7			V
ON BIAS CURRENT	VIN = 12V, ENABLE = 5V, UNLOADED	1, 2, 3	23		55	mA
	VIN = 3V, ENABLE = 1V	1, 2, 3	1.1	1.37	1.7	mA
STANBY BIAS CURRENT	VIN = 12V, ENABLE = 1V	1, 2, 3	1		1.6	mA
	VIN = 3V, ENABLE = 0V	1, 2, 3	5	25	40	µA
OFF BIAS CURRENT	VIN = 12V, ENABLE = 0V	1, 2, 3	45	105	165	µA
VREF	VIN = 5V, VOUT = VREF	1, 2, 3	594.5	600	603.5	mV
LINE REG	ΔVIN = 3V TO 16V, VOUT = 2.5V, Io = 0.0A	1, 2, 3		±0.5		%
LOAD REG	ΔIo = 0A TO 3A	1, 2, 3		±1.0		%
POSITIVE PEAK CURRENT LIMIT (2)	VIN = 3V	1, 2, 3	4.3	5.3	6.1	A
	VIN ≥ 5V	1, 2, 3	4	5	6	A
	VIN = 12V	1, 2, 3	4.9	6.2	7.3	A
NEGATIVE PEAK CURRENT LIMIT (2)		1, 2, 3	-5.7	-4.9	-3.7	A
		1, 2, 3	-5.7	-4.7	-3.7	A
		1, 2, 3	-5.8	-4.8	-3.6	A
OUTPUT CURRENT LIMIT	DELTA VOUT = -10%	1, 2, 3		3.4		A
OUTPUT RIPPLE VOLTAGE	20MHz BANDWIDTH	1, 2, 3		22.5		mVpp
THERMAL SHUTDOWN (2)		-		161		°C
THERMAL RESET (2)		-		148		°C
THERMAL SHUTDOWN HYSTERESIS (2)		-		20		°C
ERROR AMP TRANSCONDUCTANCE (2)		1, 2, 3		12		S
ERROR AMP GAIN (2)		1, 2, 3	55.3	82		dB
SWITCHING FREQUENCY		4, 5, 6	450	500	550	kHz
SLOPE COMP (2)		4, 5, 6	0.1	0.13	0.16	V/µs
RISING EDGE ENABLE	ENABLE RISING EDGE TO VOUT = 10%	1, 2, 3	1.18	1.21	1.3	V
FALLING EDGE ENABLE	ENABLE FALLING EDGE TO VOUT = 90%	1, 2, 3	0.96	1.0	1.06	V
OUTPUT OVERVOLTAGE ERROR THRESHOLD (2)	VIN = 5V, FB AS % OF VREF	1, 2, 3	106	106.8	107.5	%
OUTPUT UNDERVOLTAGE ERROR THRESHOLD (2)	VIN = 5V, FB AS % OF VREF	1, 2, 3	92.25	93.2	94.25	%
OUTPUT OVERVOLTAGE FAULT (2)	VIN = 5V, FB AS % OF VREF	1, 2, 3	113.5	115	117.25	%
OUTPUT UNDERVOLTAGE FAULT (2)	VIN = 5V, FB AS % OF VREF	1, 2, 3	82.5	85	87	%
THERMAL RESISTANCE	(AVERAGE THERMAL RESISTANCE ACROSS ENTIRE DIE)	-	-	7.1	7.2	°C/W
EFFICIENCY		1, 2, 3	80%	85%	-	%

NOTES:

(1) Unless otherwise specified VIN = 12V, VOUT = 3.3V, IOUT = 1.5A
(2) Guaranteed by design. Typical parameters are representative of actual device performance but are for reference only.
(3) Internal solder reflow temperature is 220°C, do not exceed.
(4) Pre and Post Irradiation Limits at 25°C up to 100kRAD(Si) TID are identical unless otherwise specified.

APPLICATION NOTES

PIN FUNCTIONS

PGND – The PGND pins are the high-current ground reference. Connect them directly to the negative side of the PVIN decoupling capacitors. High di/dt switching currents are conducted through these pins. Provide a continuous low impedance ground path between the PGND pins, the input supply return, and the load. Avoid layouts that force load return current to cross the SGND reference path.

CASE – The CASE pin provides electrical connection to the package. The package and CASE pin are isolated from all internal circuitry.

VIN – The VIN pins are the input supply pins for all of the internal circuitry. High di/dt switching currents are conducted through these pins. Locally decouple VIN to PGND with a mix high frequency ceramic capacitors and low ESR tantalum. Provide sufficient bulk capacitance to ensure a low impedance buss and limit input voltage ripple.

EN – The EN pin serves as the Enable input. Include 10nF bypass capacitor to ground to mitigate Single Event Effects. When EN is less that 0.3V the device is in shutdown mode drawing a maximum of 190uA and placing the switching node into a high impedance state. When the Enable voltage exceeds 1V and is less than 1.2V the device enters standby mode, drawing approximately 1.7mA. When the Enable voltage exceeds 1.2V normal operation begins after the shutdown period.

PGOOD – The PGOOD pin is an output of the internal control circuitry. The open drain signal will transition to SGND when the output falls outside regulation. This transition typically occurs when VFB falls outside ±6%. Include 100pF bypass capacitor to mitigate Single Event Effects.

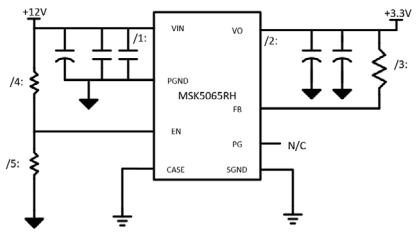
SGND – The SGND pin provides a low noise signal reference for the internal control circuitry.

FB – The FB pin is the inverting input of the error amplifier. A precision 1KΩ 0.1% 25ppm resistor is internally connected between the FB and SGND pins. The external resistor can be calculated from the following equation:

$$R_T = \frac{VO}{V_{ref}} \bullet R_B$$

Connect a resistor from VOUT to FB to complete the divider.

VOUT – The VOUT pins provide access to the output of the regulator. Refer to application circuit for recommended external capacitors.



/1: Cin: Quantity 2 C5750X7R1E226M, Quantity 1 T521V107M020ANE050

/2: Cout: Quantity 2 TBME476K035LBSZ0H00

/3: 4.42KΩ; Required for proper operation.

/4: 40.2KΩ

/5: 28KΩ

POSITIVE OVERCURRENT PROTECTION - Overcurrent protection (OCP) is provided for the sourcing and sinking output current conditions. An accurate current-sensing pilot device parallel to the upper MOSFET is used for peak current control signal and overcurrent protection. Current is sensed and monitored on the output current ripple at the most positive peak and negative valley amplitudes for the sourcing and sinking conditions. An excessive ripple current lowers the DC output current capability because of the peak detection used for OCP. OCP is triggered if the OCP threshold is exceeded in four of the eight preceding switching periods. On the 4th current peak above the OCP threshold, the device enters the fault state, stops switching, and the output is pulled low by the output loading. The device attempts to turn on again in a hiccup mode, and when the overcurrent condition goes away, the output soft starts again into a regulated output voltage. The typical sourcing OCP threshold is ~5A, ~1.7x the rated output current of 3A, providing headroom for the peak ripple current. During the soft-start period, there is an additional level of overcurrent protection of a single instance at ~6A to protect against shorted or otherwise damaged loads. When invoked, this fault goes into hiccup restart cycling until a successful restart occurs.

NEGATIVE OVERCURRENT PROTECTION - If an external source drives current into the VOUT pin, the controller attempts to regulate the output voltage by reversing its inductor current to absorb the externally sourced current. If the external source is low-impedance, it might reverse the current to an unacceptable level, and the controller initiates its negative overcurrent limit protection. The negative overcurrent protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches the negative current limit of typically -4.8A, the NOCP fault is declared, and the switching node goes into a high-z state. The IC enters into a hiccup mode to restart. There is no valley current counter on the NOCP function.

POWER GOOD - Power-Good (PG) is the output of a window comparator that continuously monitors the buck regulator output voltage. The PG output is actively held low when EN is low and during the buck regulator soft-start period. After soft-start completes, the PG pin becomes high impedance as long as the output voltage is in nominal regulation of the output voltage. When VFB is typically beyond ±6% of the nominal regulation voltage for ~5µs, the device open drain output pulls the PG output low. An external resistor from PG to a maximum of the PVIN voltage can be added for PG signaling purposes.

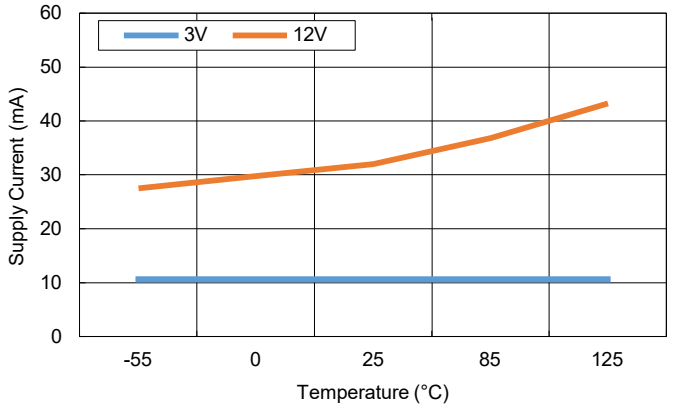
APPLICATION NOTES CONT'D

UNDERVOLTAGE LOCKOUT, ENABLE, SOFT-START, DISABLE AND SOFT-STOP - When PVIN is below the Undervoltage Lockout (UVLO) threshold, the regulator is inert until PVIN rises above the UVLO voltage of ~2.86V. The Enable pin (EN) provides three states of operation. Below the standby threshold (typically 0.68V), the device is disabled and draws a typical 105µA from PVIN. The internal VCC LDO can start up with the EN pin between a typical 1.0V and 1.2V, and the part enters a standby state. Normal switching operation and soft-start begin when the EN pin is over 1.2V. During startup, the regulator critiques for Overvoltage (OV) and Over-Temperature (OT) faults and remains idle if either fault is active. The soft-start time relates to the operating switching frequency during startup. There is a delay from enable active to switching node activity during which the regulator internal circuitries are biased. The regulator can seamlessly start into a pre-biased output, provided the output voltage is below the set regulation voltage. If the pre-biased output exceeds the regulation set point, the regulator does not initiate switching at the switch node but turns on the low-side MOSFET to pull the output down. Suppose the sinking output current reaches the negative output current limit (NOCL). In that case, it enters hiccup operation until the output is below the regulation set point and then proceeds through soft-start to switch node switching. If the sinking output current does not reach the NOCL, the regulator initiates soft-start when VOUT is pulled below the regulation set point. The device is disabled and enters the low current shutdown state when EN is < 0.3V. When a transition to a shutdown state occurs, the switching node output is forced to a hi-Z state.

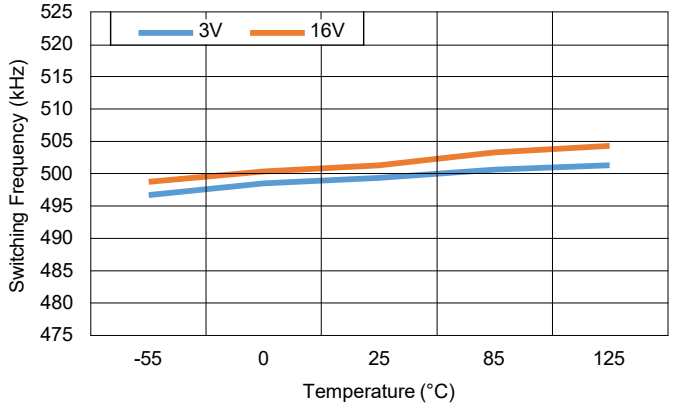
THERMAL PROTECTION - When the internal temperature reaches ~ +158°C, the regulator stops switching. After the internal temperature falls below ~ +130°C, the device resumes operation through soft-start. For continuous operation, do not exceed the +150°C junction temperature rating.

TYPICAL PERFORMANCE CURVES

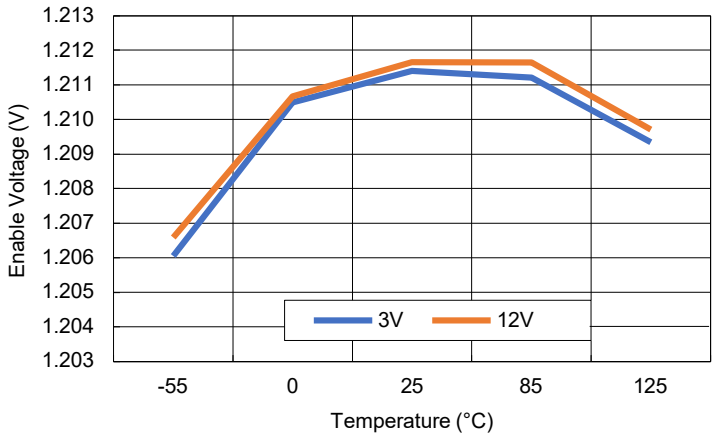
SUPPLY CURRENT
vs TEMPERATURE



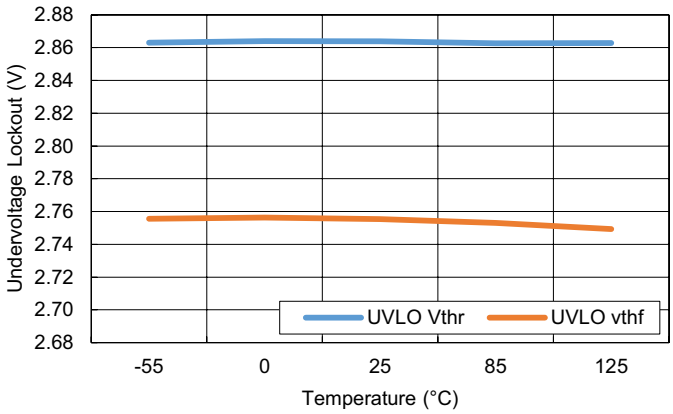
SWITCHING FREQUENCY
vs TEMPERATURE



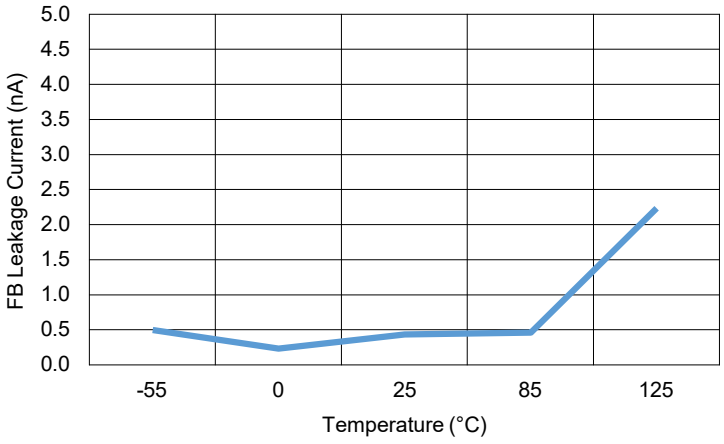
ENABLE VOLTAGE
vs TEMPERATURE



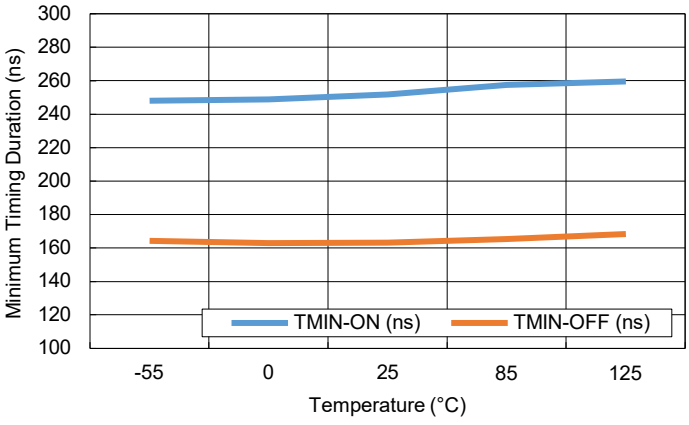
UNDERVOLTAGE LOCKOUT
vs TEMPERATURE



FEEDBACK LEAKAGE
vs TEMPERATURE

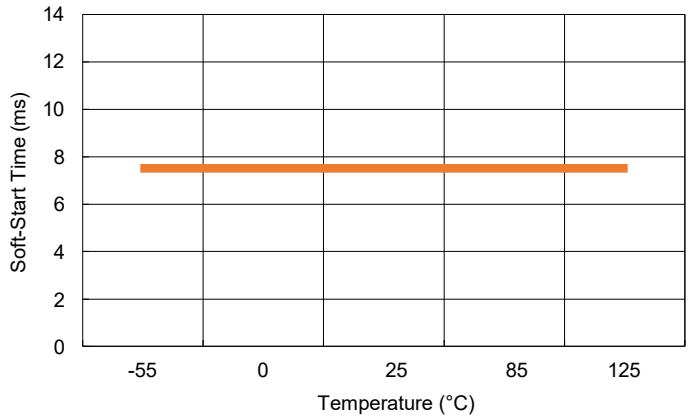


MINIMUM ON/OFF TIME
vs TEMPERATURE

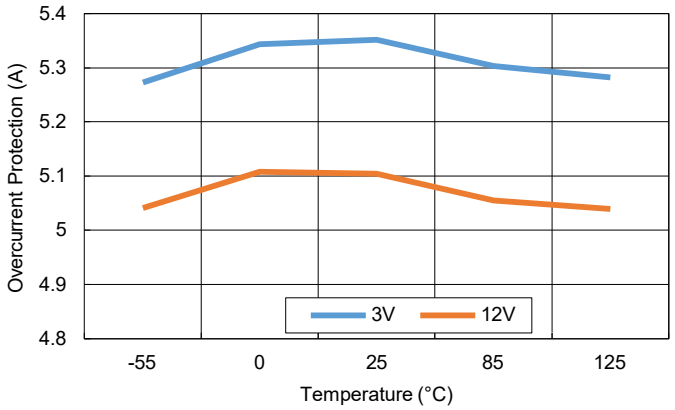


TYPICAL PERFORMANCE CURVES CONT'D

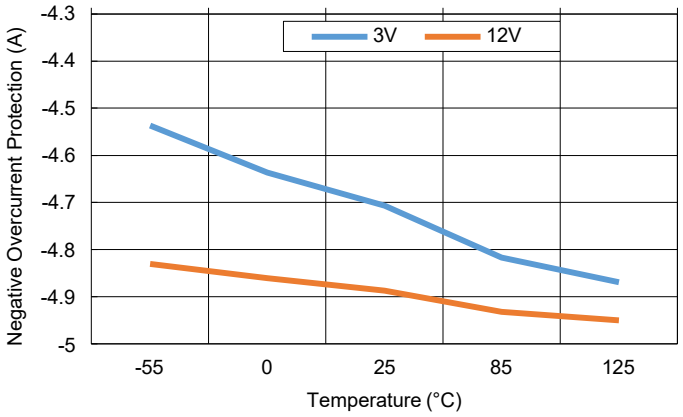
SOFT START TIME
vs TEMPERATURE



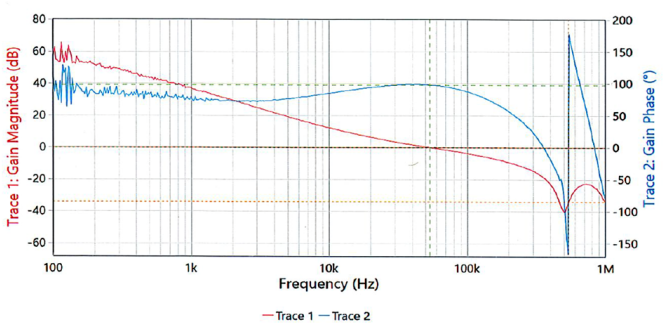
POSITIVE OVERCURRENT LIMIT
vs TEMPERATURE



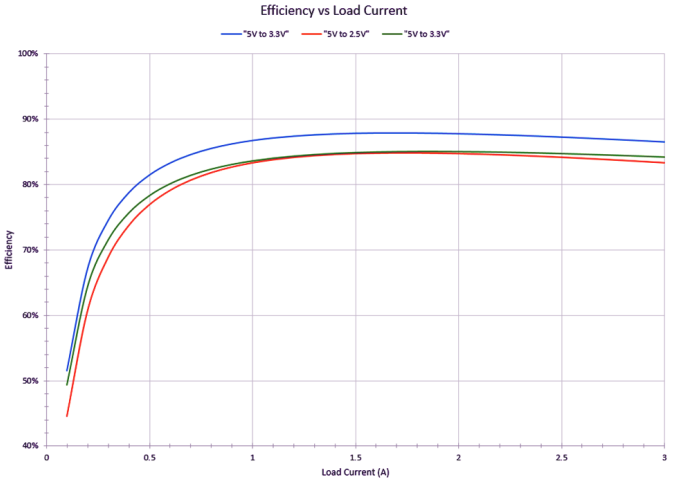
NEGATIVE OVERCURRENT LIMIT
vs TEMPERATURE

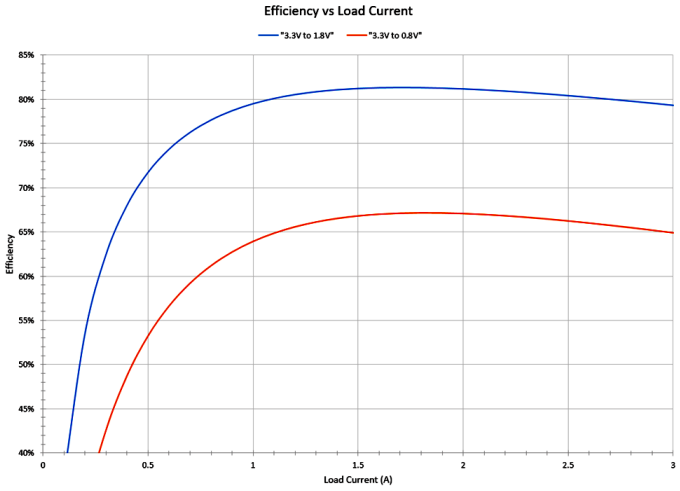


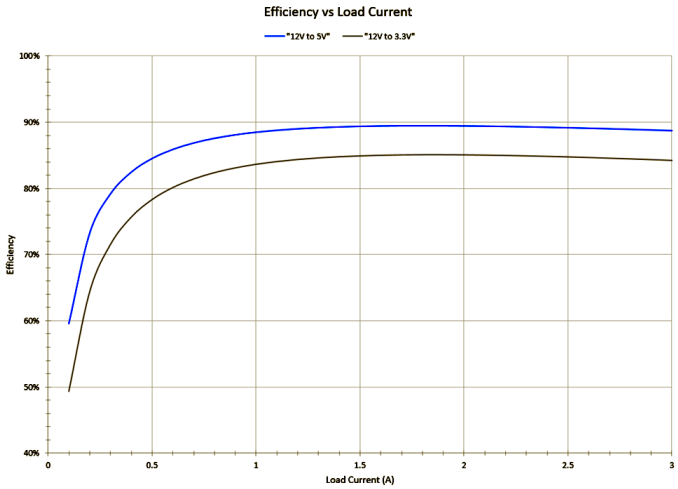
TYPICAL PERFORMANCE CURVES CONT'D



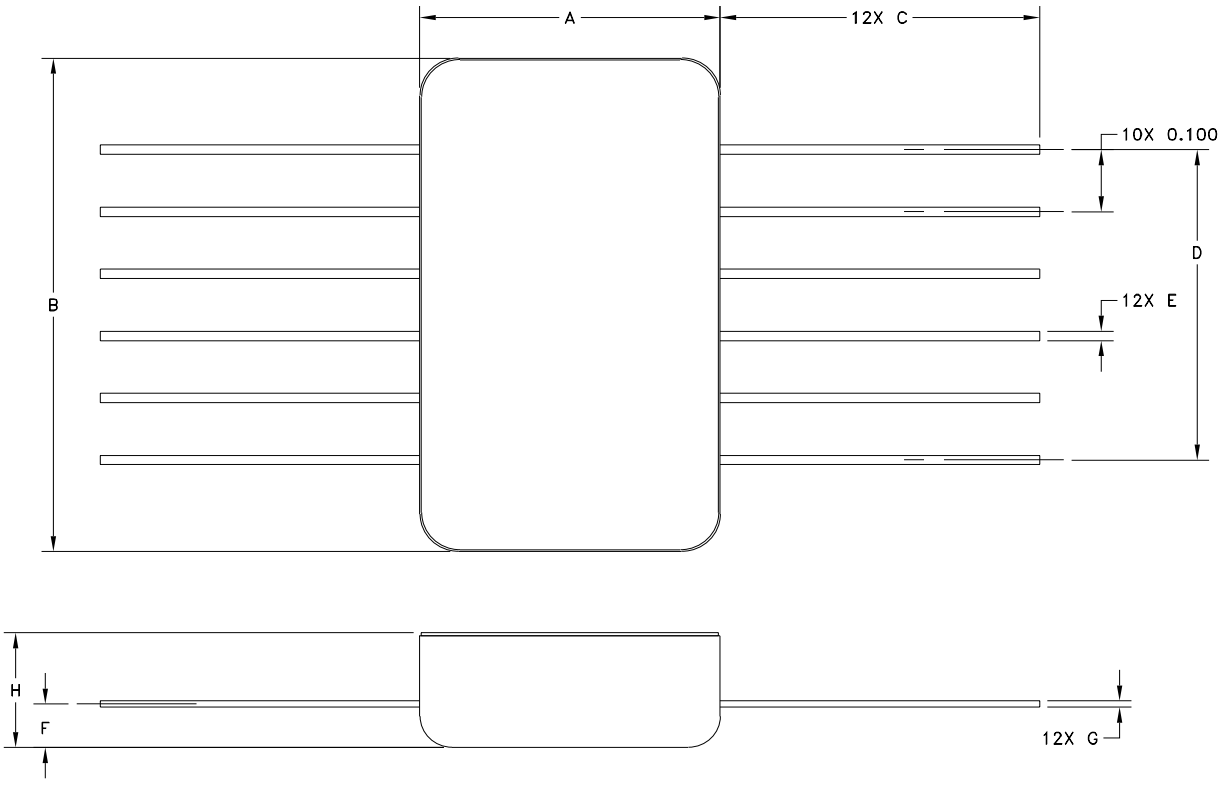
	Cursor 1	Cursor 2
Frequency	54.245 kHz	543.054 kHz
Trace 1	**Magnitude (dB)**	**Magnitude (dB)**
Measurement	0 dB	-33.889 dB
Trace 2	**Phase (°)**	**Phase (°)**
Measurement	98.04 °	0 °







MECHANICAL SPECIFICATIONS



REF	MIN	MAX
A	0.460	0.480
B	0.785	0.805
C	0.500	———
D	0.495	0.505
E	0.012	0.018
F	0.050	0.075
G	0.009	0.011
H	———	0.175

WEIGHT = TBD GRAMS MAX

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

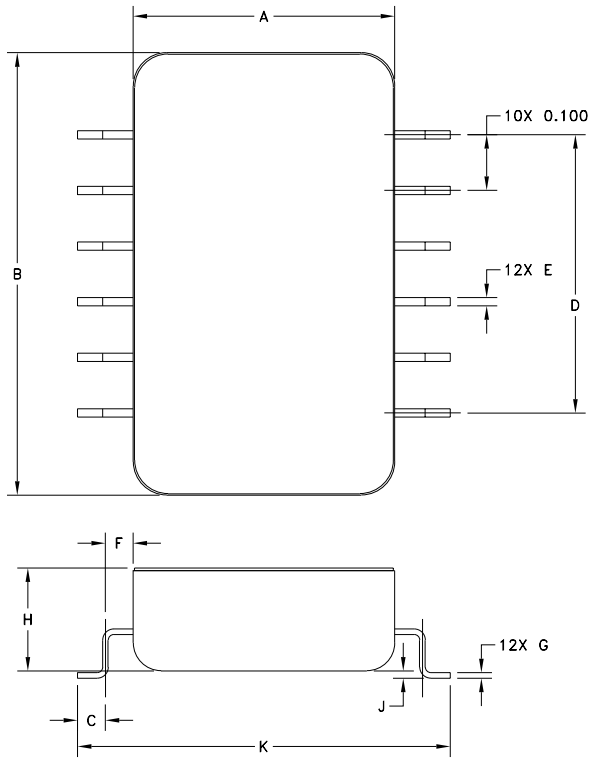
MSK5065 _ RH _

LEAD CONFIGURATIONS
BLANK= STRAIGHT

RADIATION HARDENED

SCREENING
EDU=NON-RAD HARD ENG UNITS
BLANK= INDUSTRIAL; H=MIL-PRF38534 CLASS H;
K=MIL-PRF-38534 CLASS K

GENERAL PART NUMBER



REF	MIN	MAX
A	0.460	0.480
B	0.785	0.805
C	0.045	0.055
D	0.495	0.505
E	0.012	0.018
F	0.050 REF	
G	0.009	0.011
H	———	0.175
J	0.009	0.018
K	0.650	0.690

NOTE: DIMENSION "J" IS MEASURED FROM BOTTOM OF PIN TO BOTTOM OF CASE

WEIGHT = TBD GRAMS MAX

ALL DIMENSIONS ARE SPECIFIED IN INCHES

ORDERING INFORMATION

MSK5065 _ RH G

LEAD CONFIGURATIONS
G=GULL WING

RADIATION HARDENED

SCREENING
EDU=NON-RAD HARD ENG UNITS
BLANK= INDUSTRIAL; H=MIL-PRF38534 CLASS H;
K=MIL-PRF-38534 CLASS K

GENERAL PART NUMBER

REVISION HISTORY

REV	STATUS	DATE	DESCRIPTION
Preliminary	Released	09/23	Initial Release