



1.8 – 2.8 GHz Group Delay Compensator

Description:

The XGDC1828F-01S is a 1.8 – 2.8 GHz group delay compensator rated for 15 Watts average power, with a 12dB peak-to-average performance. Available in a user-friendly Xinger-style surface-mount package. This device is engineered specifically for wideband Doherty amplifier applications in 4G LTE, 5G and emerging 6G wireless communication systems, this device is typically placed after a hybrid coupler splitter on the input side of the power amplifier devices. It effectively compensates for the group delay mismatch between the hybrid splitter and the transmission line Doherty combiner, thereby enhancing the efficiency of the wideband Doherty amplifier.



Parts have been subjected to rigorous component qualification testing and they are manufactured using materials with coefficients of thermal expansion (CTE) compatible with common substrates such as FR4, RF-35, RO4350 and polyimide. Produced with 6 of 6 RoHS compliant tin immersion finish.

Features:

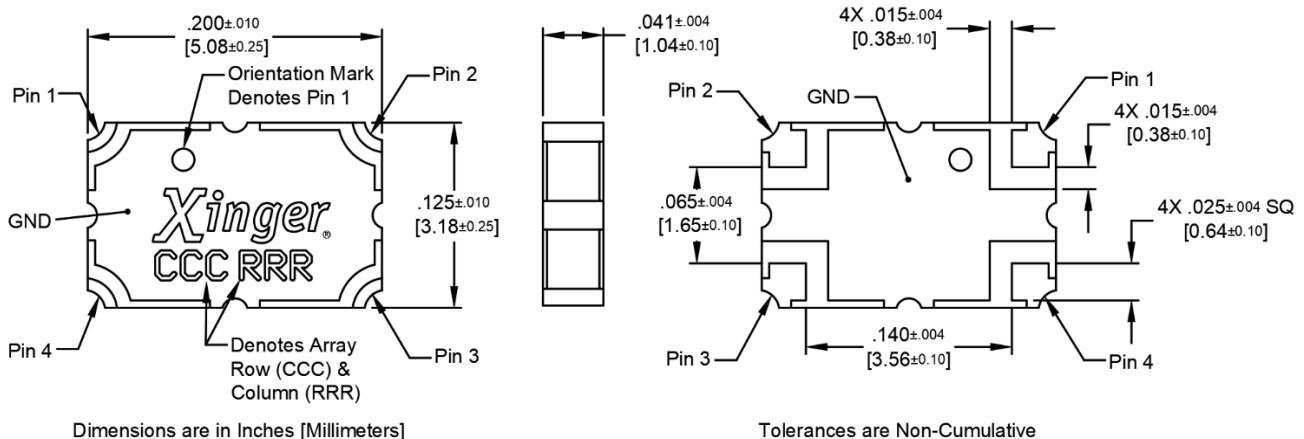
- 1.8-2.8 GHz
- 5mm x 3mm package
- 4G LTE, 5G and emerging 6G applications
- High Isolation (>35dB)
- Power 15W (AVG)
- Surface Mountable
- Production Friendly
- Tape and Reel
- RoHS Compliant
- Made in the USA

Electrical Specifications*:

Frequency	Isolation	Insertion Loss	Return Loss
GHz	dB Min	dB Max	dB Min
1.8 - 2.8	35	0.55	20
Mean Delay Balance	Phase Balance @ f _c	Power	Operating Temp.
ns	Degrees @ 2.0GHz	AVG Watts @ 105°C	°C
0.109 ± 0.02	± 6°	15	-55 to +150

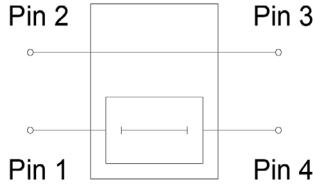
*Specification based on performance of unit properly installed on microstrip printed circuit boards with 50-ohm impedance. Specifications are subject to change without notice.

Mechanical Outline:



Pin Configuration:

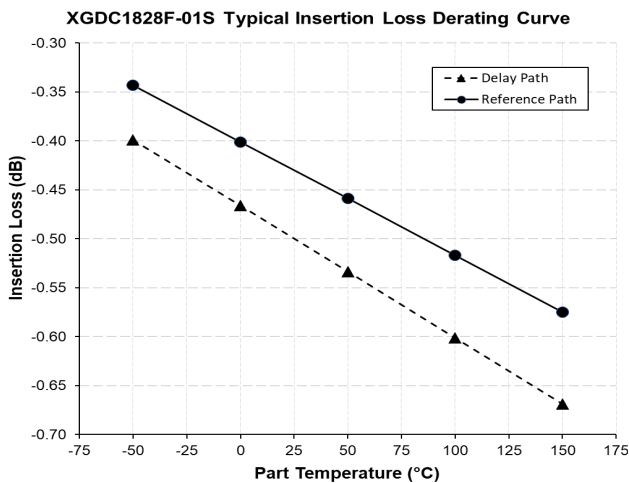
The component has an orientation marker to denote Pin 1. Once port one has been identified, the other ports are known automatically. Please see the chart below for clarification:



Pin 1	Pin 2	Pin 3	Pin 4
Delayed Path Input	Reference Path Input	Reference Path Output	Delayed Path Output
Delayed Path Output	Reference Path Output	Reference Path Input	Delayed Path Input

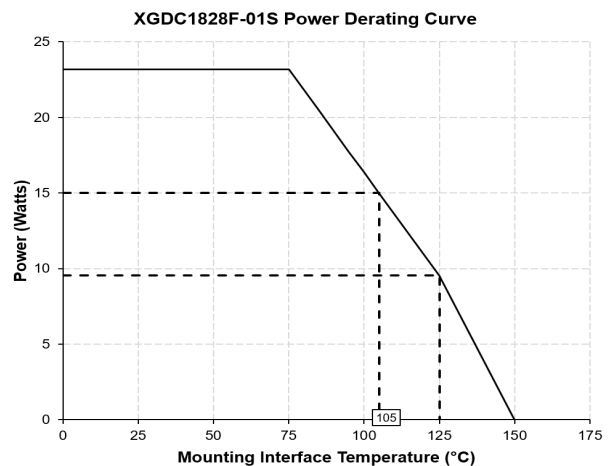
*The actual phase or amplitude at a given frequency for all ports can be seen in our de-embedded s-parameters, that can be downloaded at www.ttm.com.

Insertion Loss and Power Derating Curves:



Insertion Loss Derating:

The insertion loss, at a given frequency, of the component is measured at 25°C and then averaged. The measurements are performed under small signal conditions (i.e. using a Vector Network Analyzer). The process is repeated at -55°C, 105°C and 150°C. A best-fit line for the measured data is computed and then plotted from -55°C to 150°C.



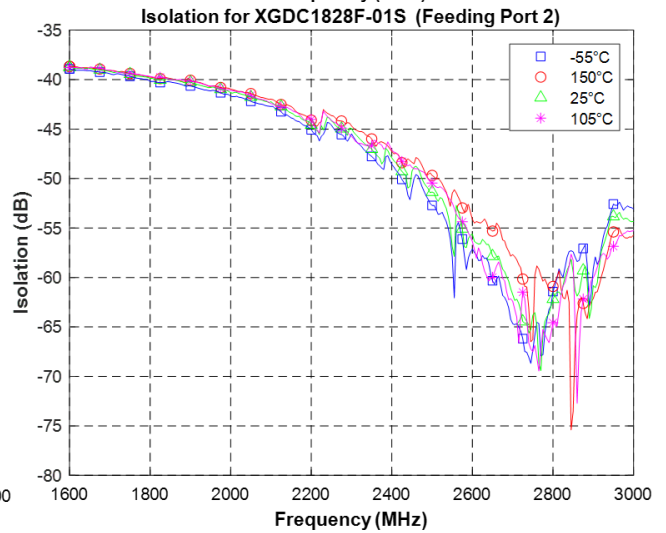
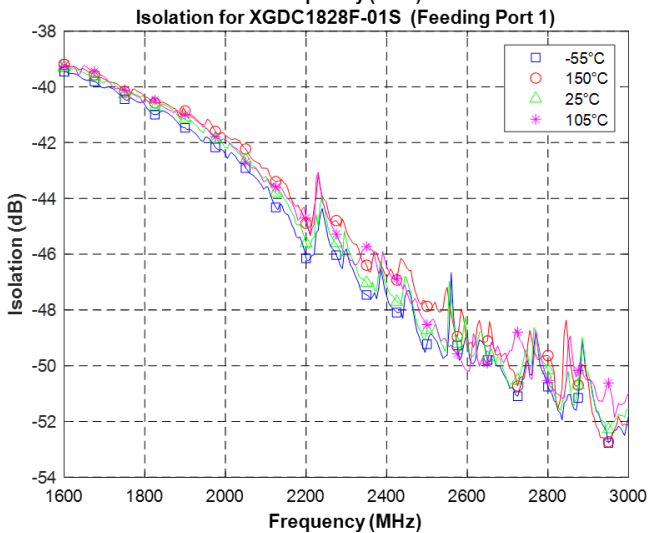
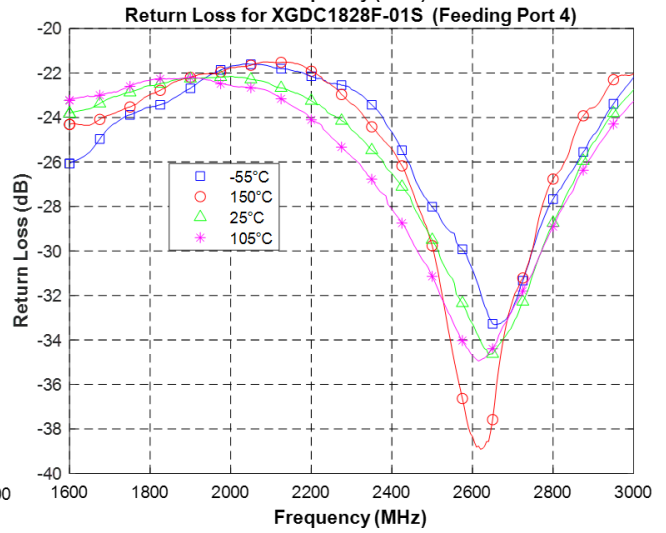
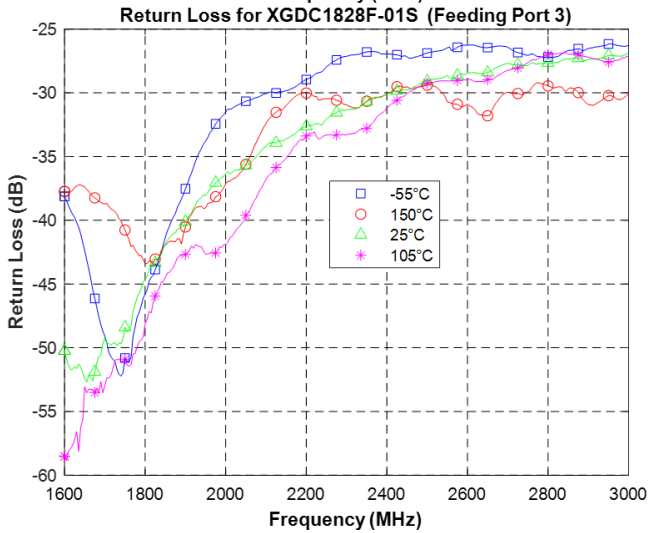
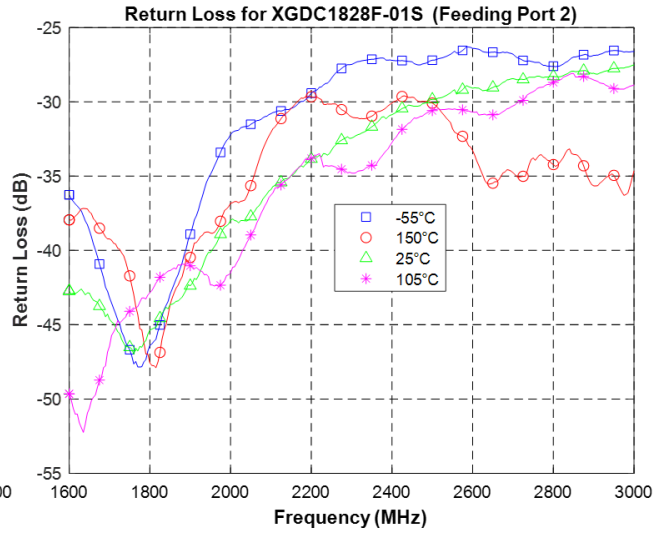
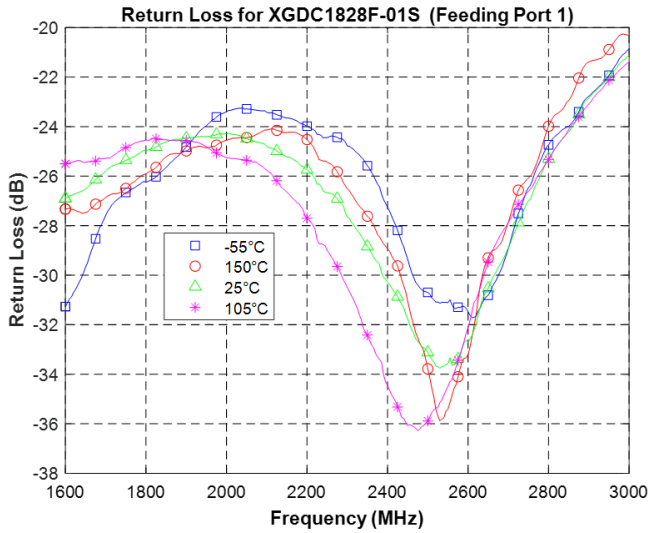
Power Derating:

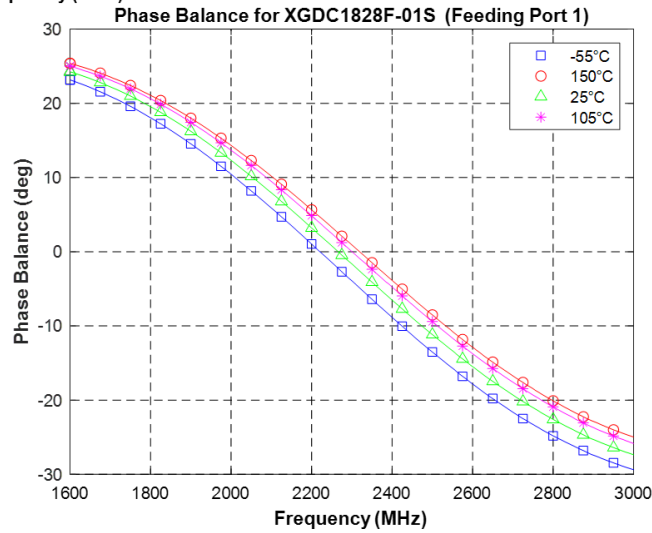
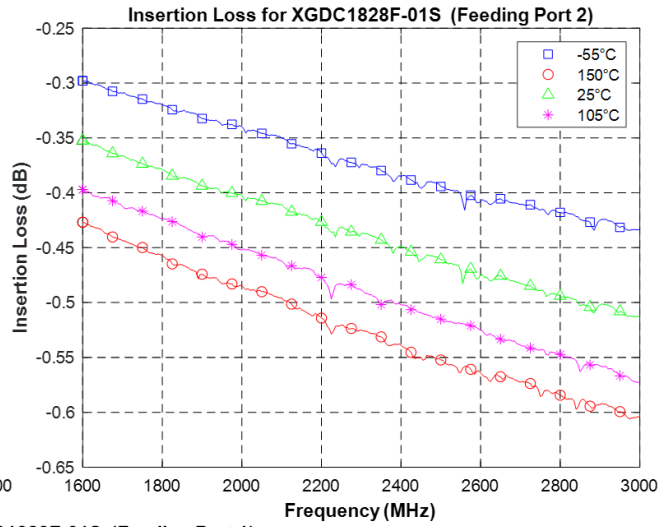
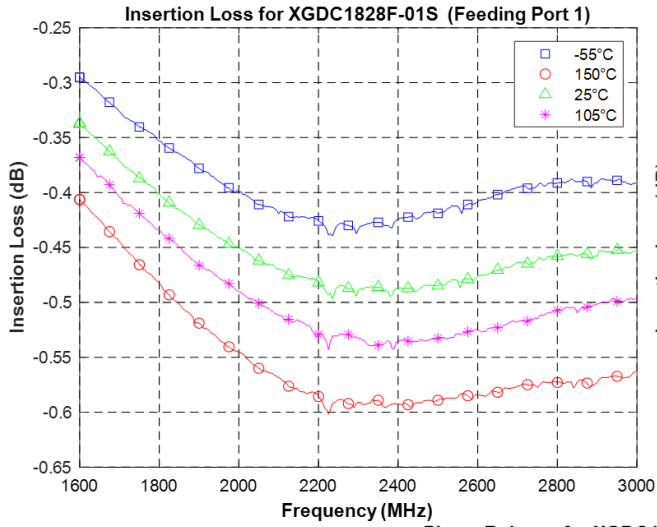
The power handling and corresponding power derating plots are a function of the thermal resistance, mounting surface temperature (base plate temperature), maximum continuous operating temperature of the component, and the thermal insertion loss. The thermal insertion loss is defined in the Power Handling section of the data sheet.

As the mounting interface temperature approaches the maximum continuous operating temperature, the power handling decreases to zero.

If mounting temperature is greater than 105°C, the component will perform reliably as long as the input power is derated to the curve above.

Typical Temperature Performance Plots:



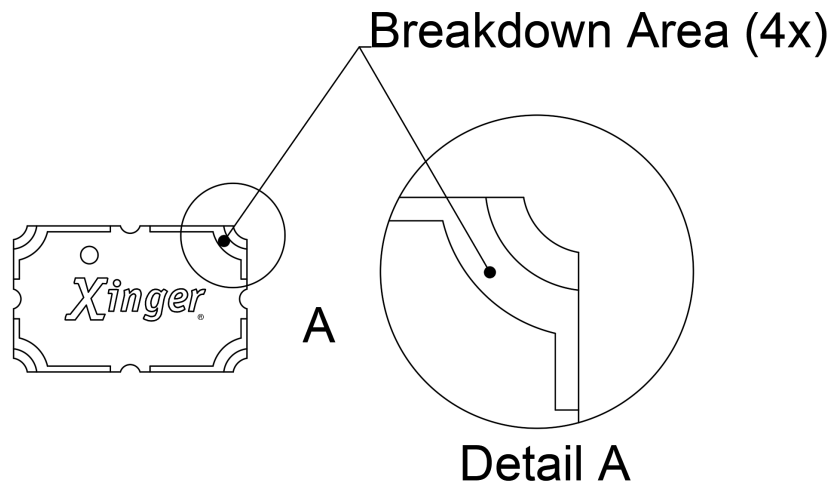


Definition of Measured Specifications:

Parameter	Definition	Mathematical Representation
Return Loss	Impedance mismatch in a 50Ω system	$-20 \times \log_{10}(S_{nn}), n = 1,2,3,4$
Insertion Loss	Signal power loss passing through the reference path or the delayed path	$-20 \times \log_{10}(S_{32})$ $-20 \times \log_{10}(S_{41})$
Isolation	Signal power leakage between reference path and delayed path	$-20 \times \log_{10}(S_{31})$ $-20 \times \log_{10}(S_{42})$
Phase Balance	The phase difference between reference path and delayed path	$Phase(S_{41}) - Phase(S_{32})$
Group Delay Balance	The group delay difference between reference path and delayed path	$gd(S_{41}) - gd(S_{32})$
Mean Group Delay Balance	Average of the group delay balance over a frequency band	$Average(gd(S_{41}(\omega)) - gd(S_{32}(\omega)))$

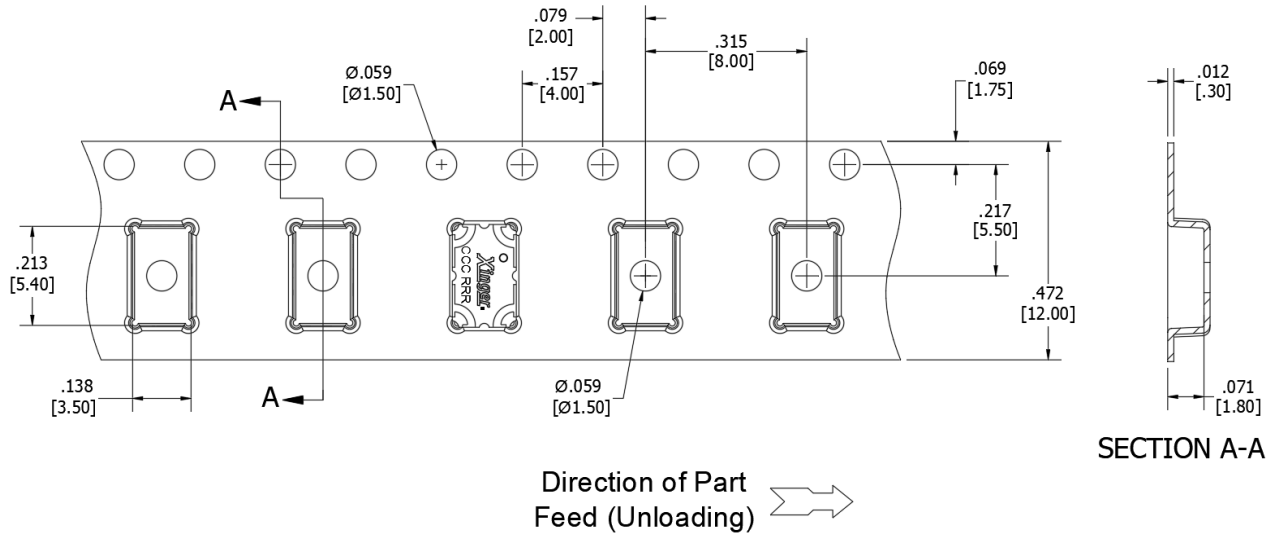
Peak Power Handling

High-Pot testing of these components during the qualification procedure resulted in a minimum breakdown voltage of 1.20 Kv (minimum recorded value). This voltage level corresponds to a breakdown resistance capable of handling at least 12dB peak over average power levels, for very short durations. The breakdown location consistently occurred across the air interface at the component contact pads (see illustration below). The breakdown levels at these points will be affected by any contamination in the gap area around these pads. These areas must be kept clean for optimum performance. It is recommended that the user test for voltage breakdown under the maximum operating conditions and over worst-case modulation induced power peaking. This evaluation should also include extreme environmental conditions (such as high humidity).



Packaging and Ordering Information:

Parts are available in reels. Packaging follows EIA 481 for reels. Parts are oriented in tape and reel as shown below. Tape and reel is available in 4000 pcs per reel.



Dimensions are in Inches [Millimeters]

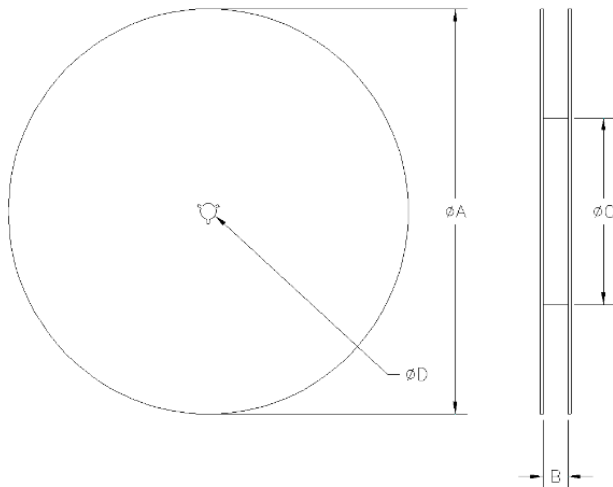


TABLE 1: 4000 pc REEL DIMENSIONS: inches [mm]

ØA	13.0 [330.00]
B	0.472 [12.00]
ØC	4.017 [102.03]
ØD	0.512 [13.00]

Part Naming Convention

XGDC 1828 F - 01 S

Function & Family	Frequency	Package Size	Group Delay Target	Finish
XGDC = Xinger Group Delay Compensator	1828 = typ freq range 1.8 to 2.8 GHz	F = 0.200" x 0.125"	01 = ~1 ns	S = Immersion Tin

Contact us:
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